

MODEL NAME : **AAM00**

PCB NO : **LA-C361P**

BOM P/N :

Dell/Compal Confidential

Schematic Document

SKYLAKE-H

2014-05-22

Rev: 0.0 (M00)

@ : Nopop Component

CONN@ : Connector Component

R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB

TPM@ : TPM function

EMC@ : Pop of EMI parts

VRAMS@ : Samsung GDDR5 for GPU

VRAMH@ : Hynix GDDR5 for GPU

VRAMM@ : Micron GDDR5 for GPU

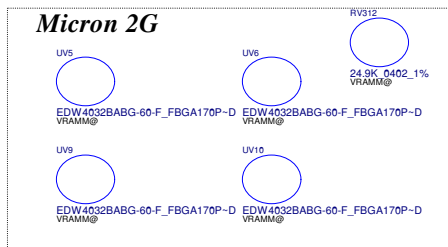
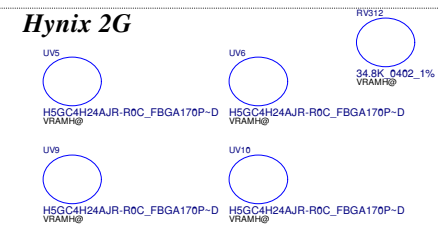
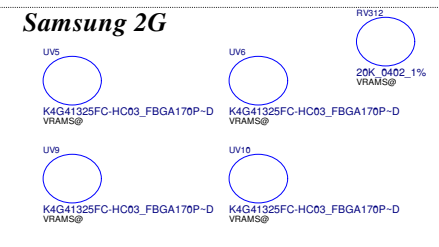
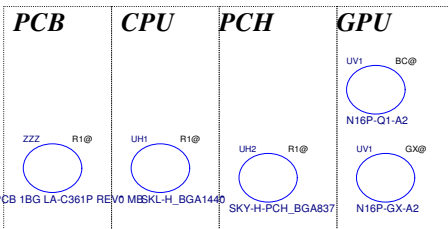
BreakDown@ : for measure power consumption

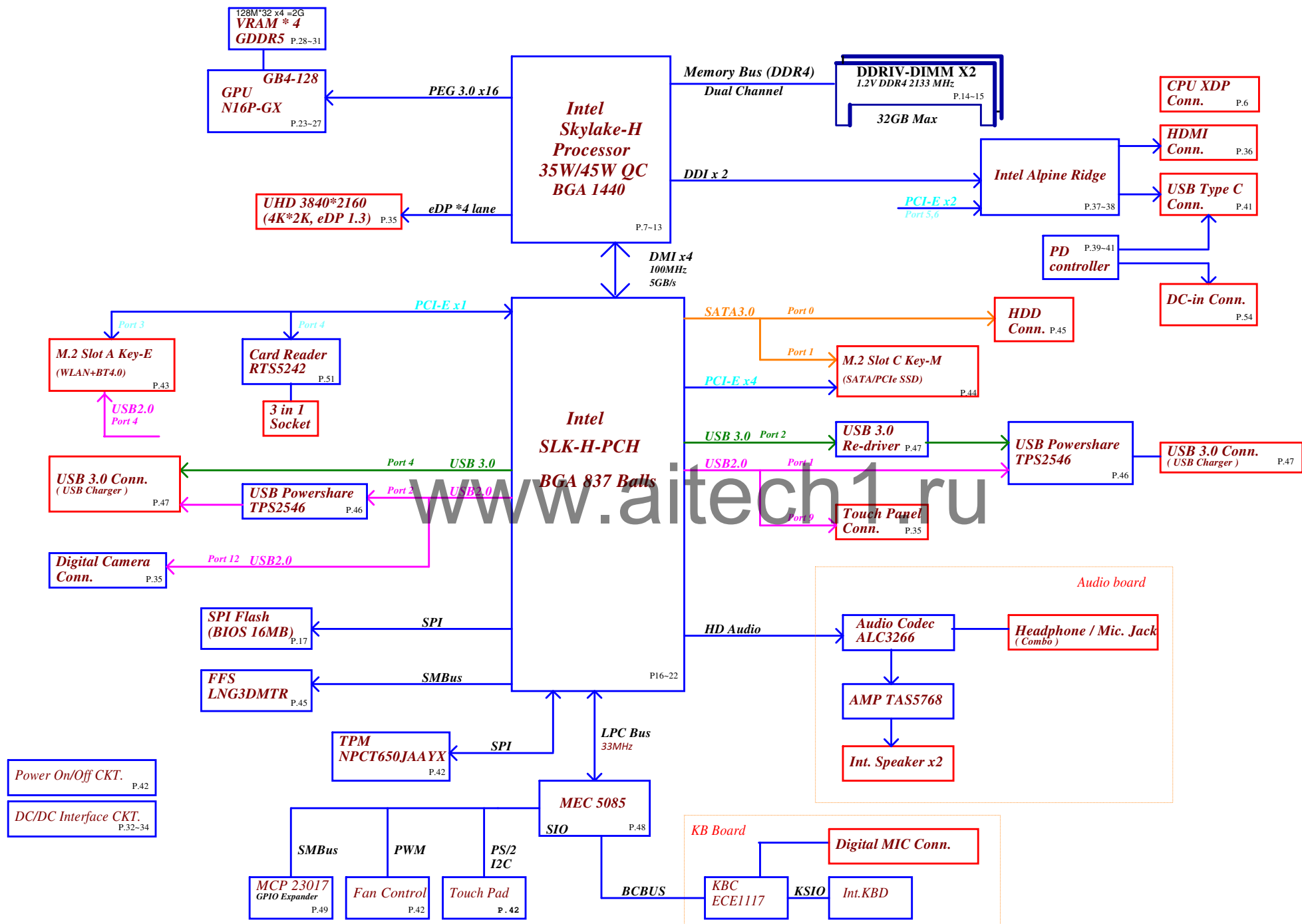
CSMB@ : CSMB sku

BC@ : BC sku (GPU N16P-Q1)

GX@ : GPU N16P-GX

UMA@ / DIS@ : UMA/DIS

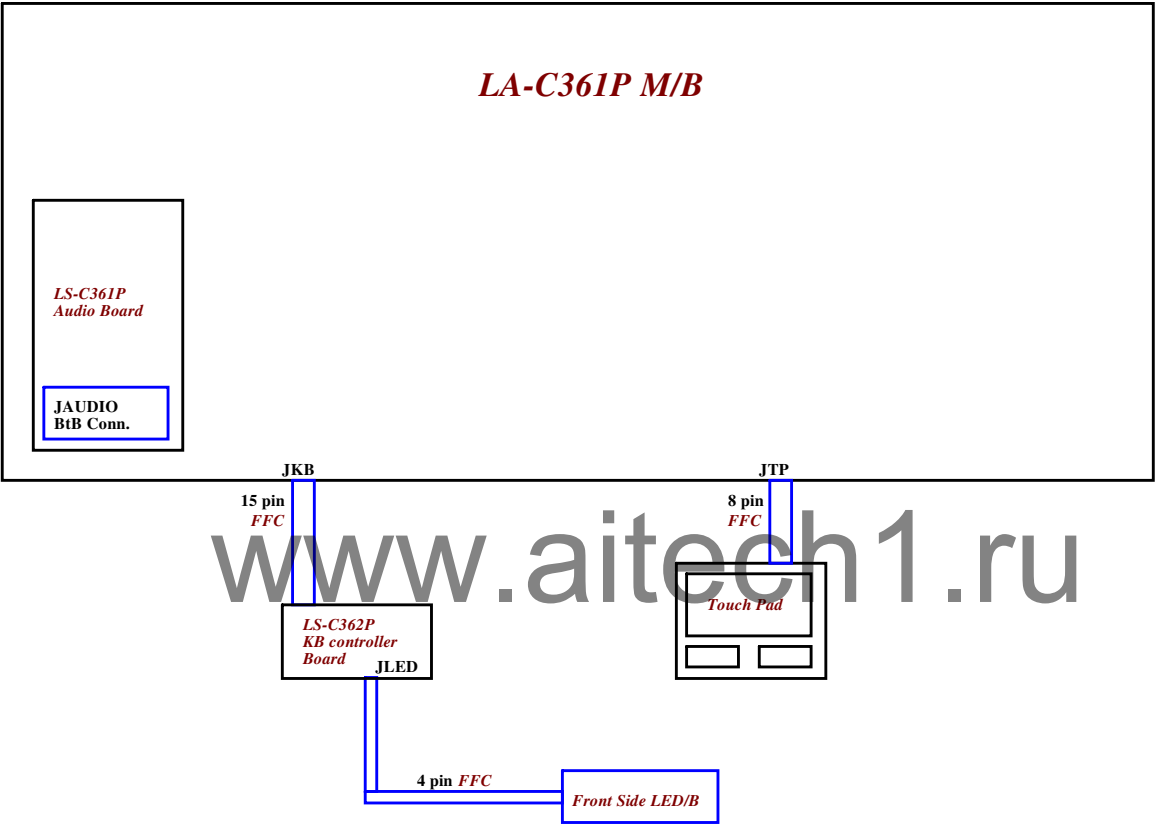




Compal Confidential

Project Code : AAM00

File Name :



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Board ID	Resistor
X00	N/A
X01	
X02	
X03	
A00	

USB3	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA



DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

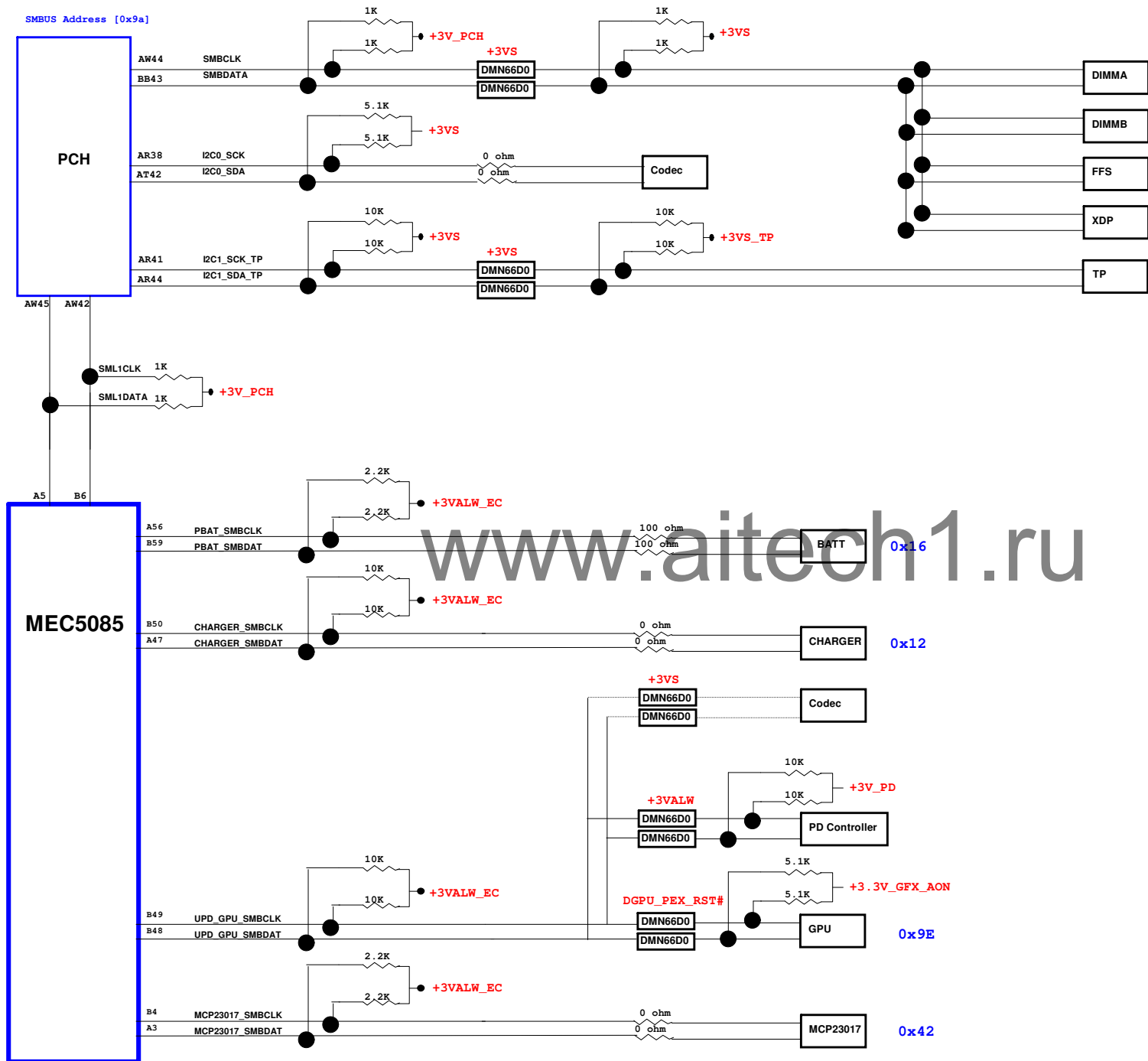
LPC	DESTINATION
LPC0	MEC5085
LPC1	DEBUG PORT

PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	CARD READER	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None	SATA	DESTINATION
Lane 9	SSD	0A	SSD
Lane 10	SSD	1A	N/A
Lane 11	SSD	N/A	N/A
Lane 12	SSD	N/A	N/A
Lane 13	None	0B	None
Lane 14	None	1B	HDD
Lane 15	Alpine Ridge	2	None
Lane 16		3	None

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

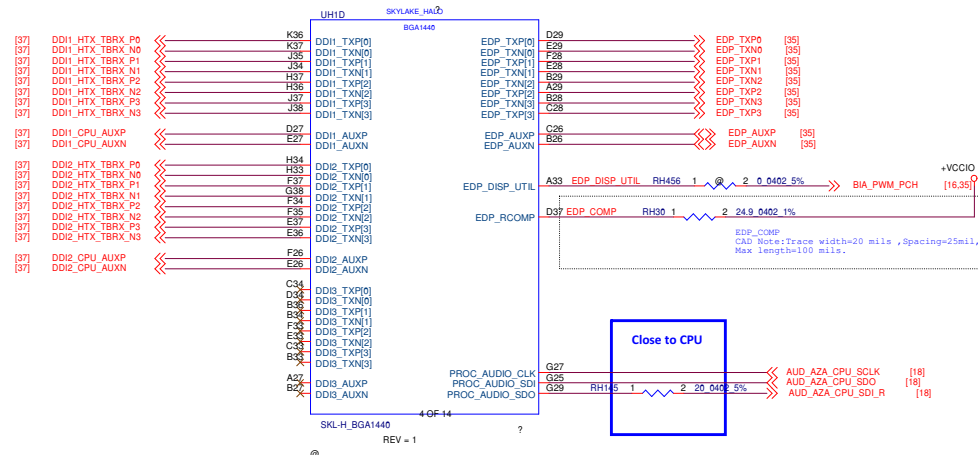
Symbol Note :

 : means Digital Ground
  : means Analog Ground

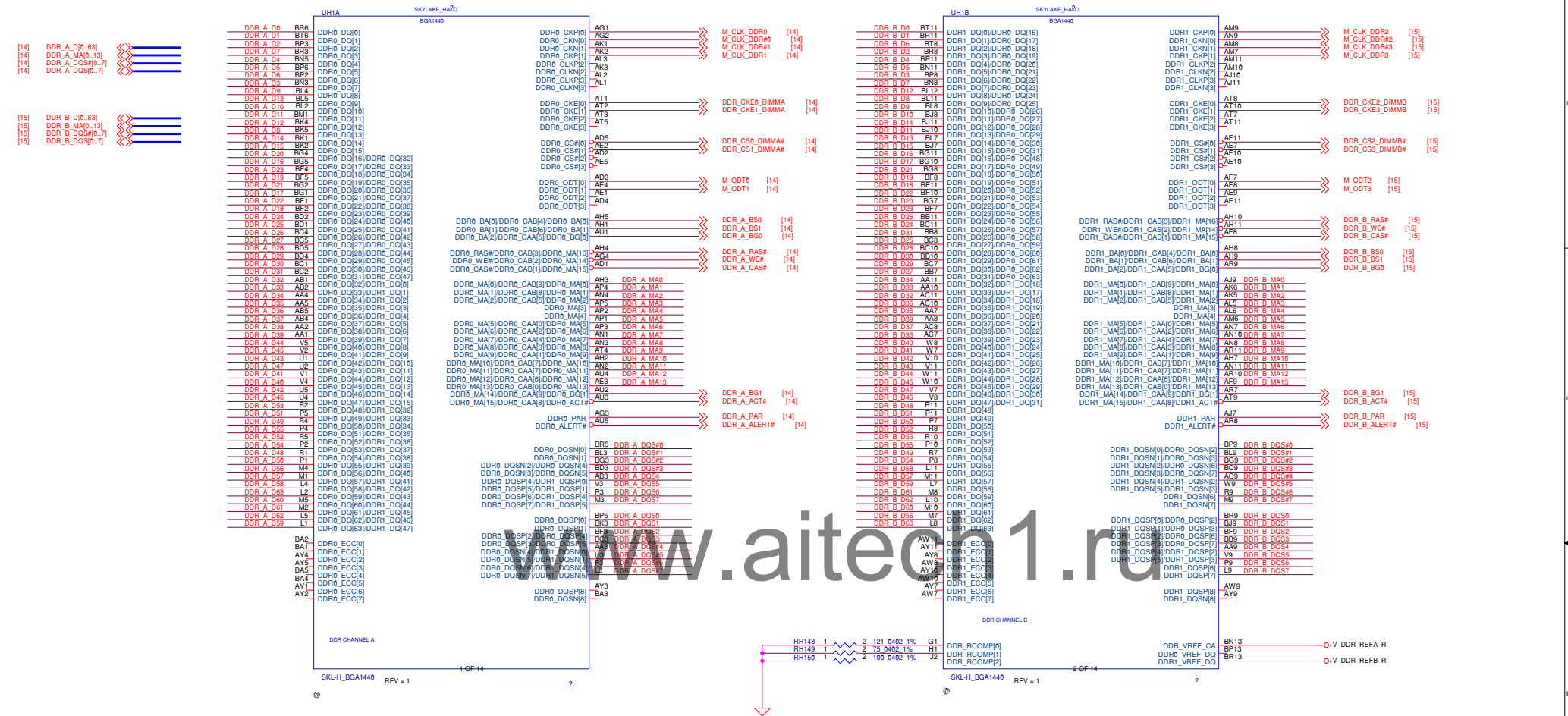


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[23] PEG_HTX_C_GRX_P10_15] << PEG_HTX_C_GRX_P10_15]
[23] PEG_HTX_C_GRX_N10_15] << PEG_HTX_C_GRX_N10_15]
[23] PEG_GTX_C_HRX_P10_15] >> PEG_GTX_C_HRX_P10_15]
[23] PEG_GTX_C_HRX_N10_15] >> PEG_GTX_C_HRX_N10_15]



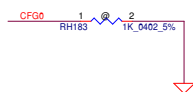
Interleave



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				Size	Document Number	Rev
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CFG Straps for Processor

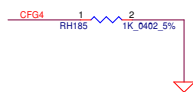
Stall reset sequence after PCU PLL lock until de-aserted	
CFG0	<p>* 1 = (Default) Normal Operation; No stall.</p> <p>0 = Stall.</p>



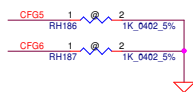
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



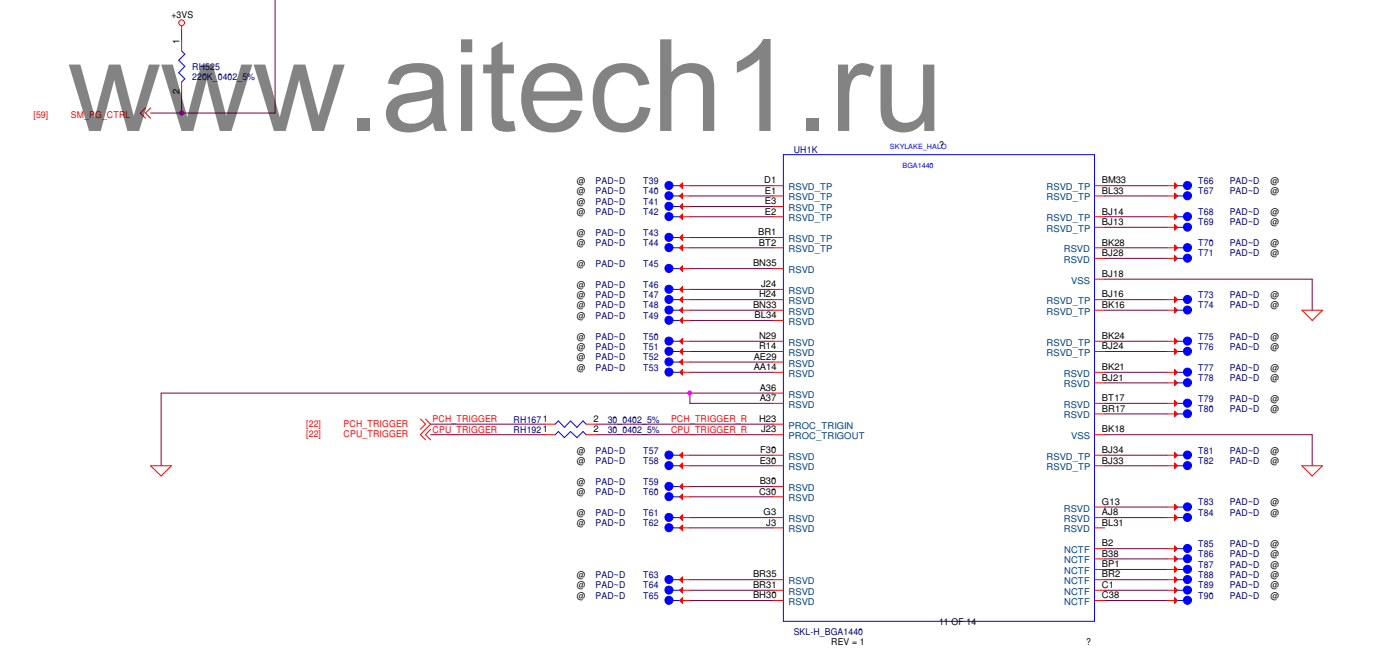
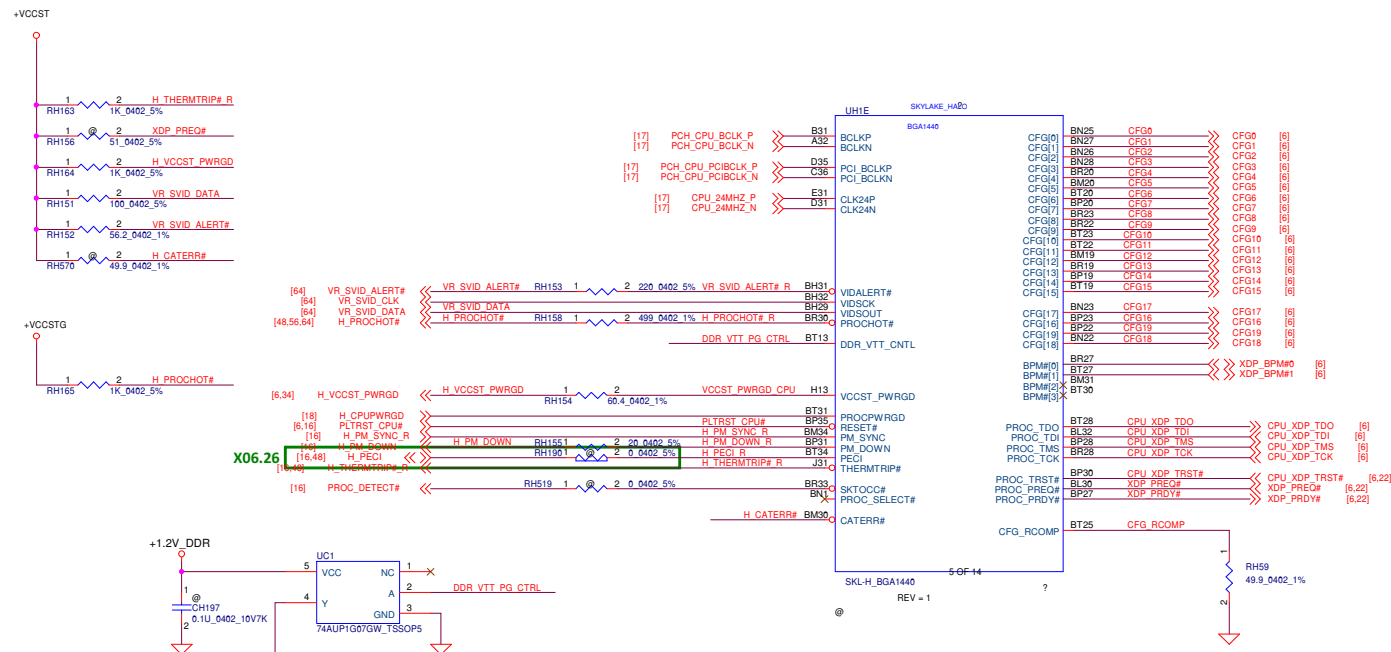
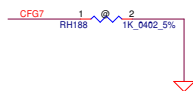
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



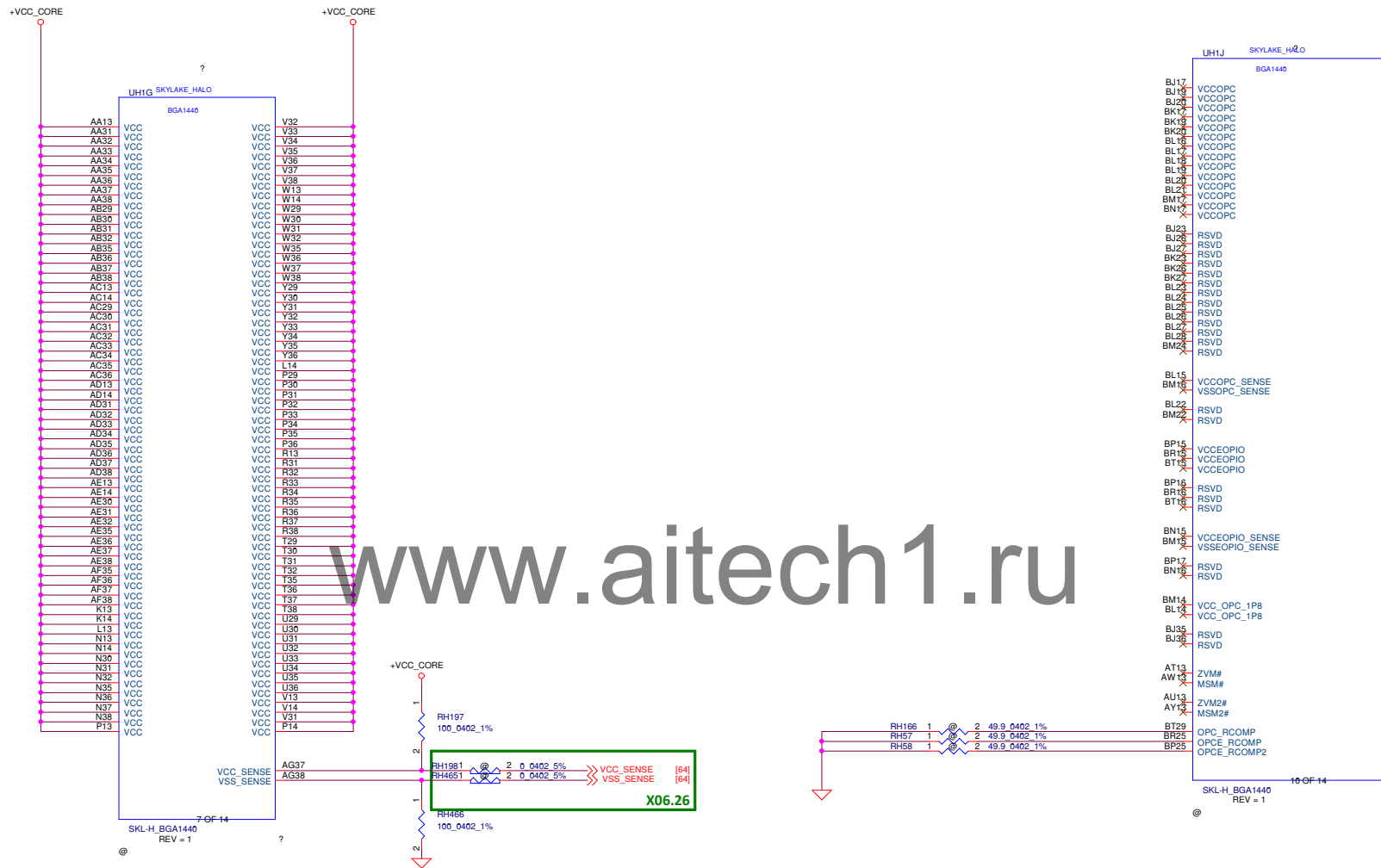
PCIe Port Bifurcation Straps	
CFG[6:5]	<p>★11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8, x4, x4 - Device 1 functions 1 and 2 enabled</p>



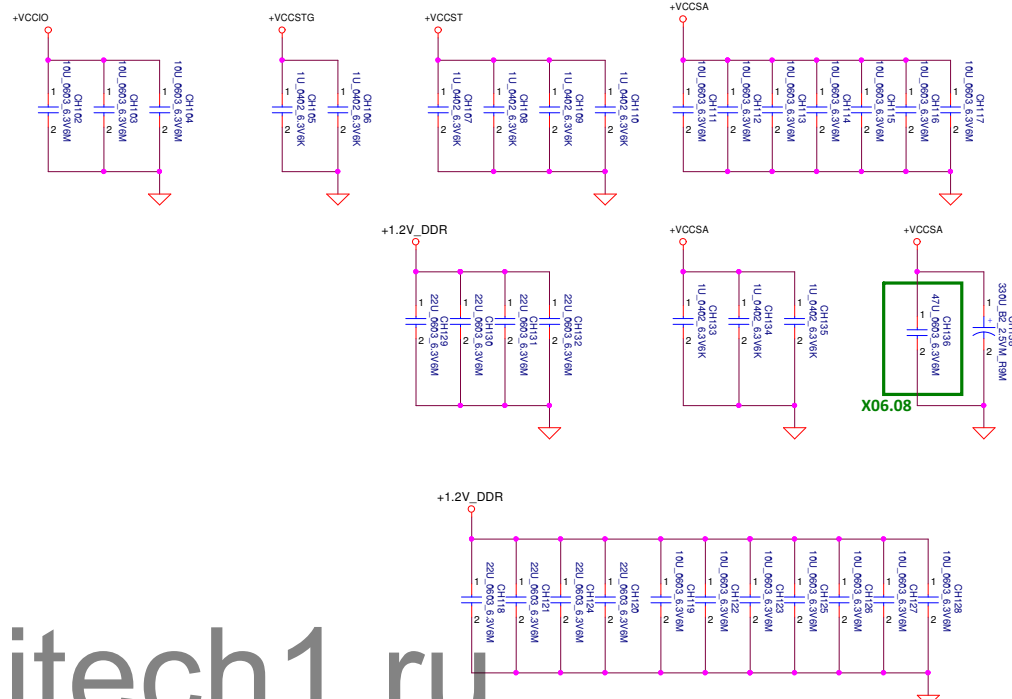
PEG DEFER TRAINING	
CFG7	<p>★ 1: (Default) PEG Train immediately following xxRESET de assertion</p> <p>0: PEG Wait for BIOS for training</p>



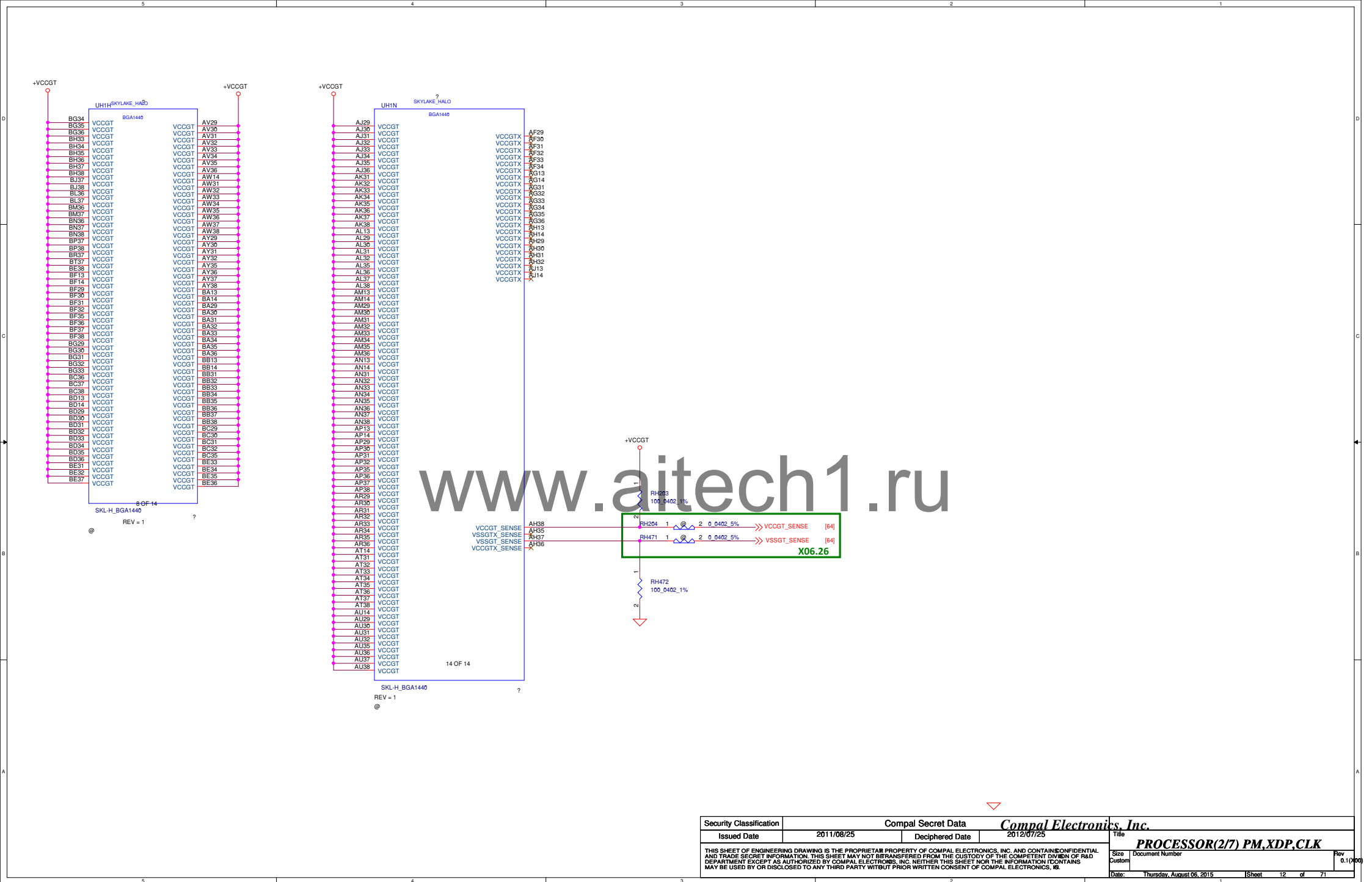
Security Classification	Compal Secret Data		<i>Compal Electronics, Inc.</i> PROCESSOR(47) RSVD.CFG	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title PROCESSOR(47) RSVD.CFG
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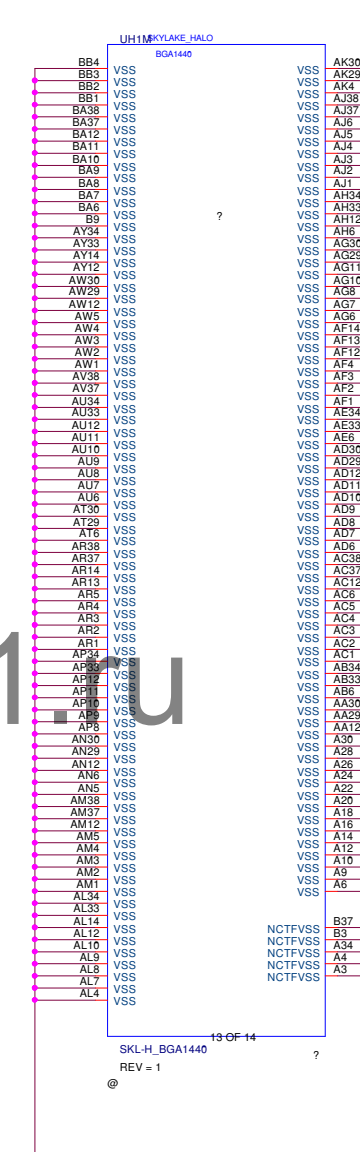
Security Classification		Compal Secret Data		Title	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Doc Number	PROCESSOR(5/7) PWR,BYPASS
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The schematic diagram illustrates the power supply section of the PCB, featuring two +1.2V DDR power planes. The top plane is connected to a +1.2V DDR input and contains capacitors CD78 through CD89. The bottom plane is also connected to a +1.2V DDR input and contains capacitors CD90 through CD101. A 0.1uF capacitor CD11 is connected between the two planes.

Top Plane Components:

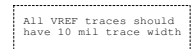
- CD78: 1uF, 0.003, 5VWV
- CD79: 1uF, 0.003, 5VWV
- CD80: 1uF, 0.003, 5VWV
- CD81: 1uF, 0.003, 5VWV
- CD82: 1uF, 0.003, 5VWV
- CD83: 1uF, 0.003, 5VWV
- CD84: 1uF, 0.003, 5VWV
- CD85: 1uF, 0.003, 5VWV
- CD86: 1uF, 0.003, 5VWV
- CD87: 1uF, 0.003, 5VWV
- CD88: 1uF, 0.003, 5VWV
- CD89: 1uF, 0.003, 5VWV

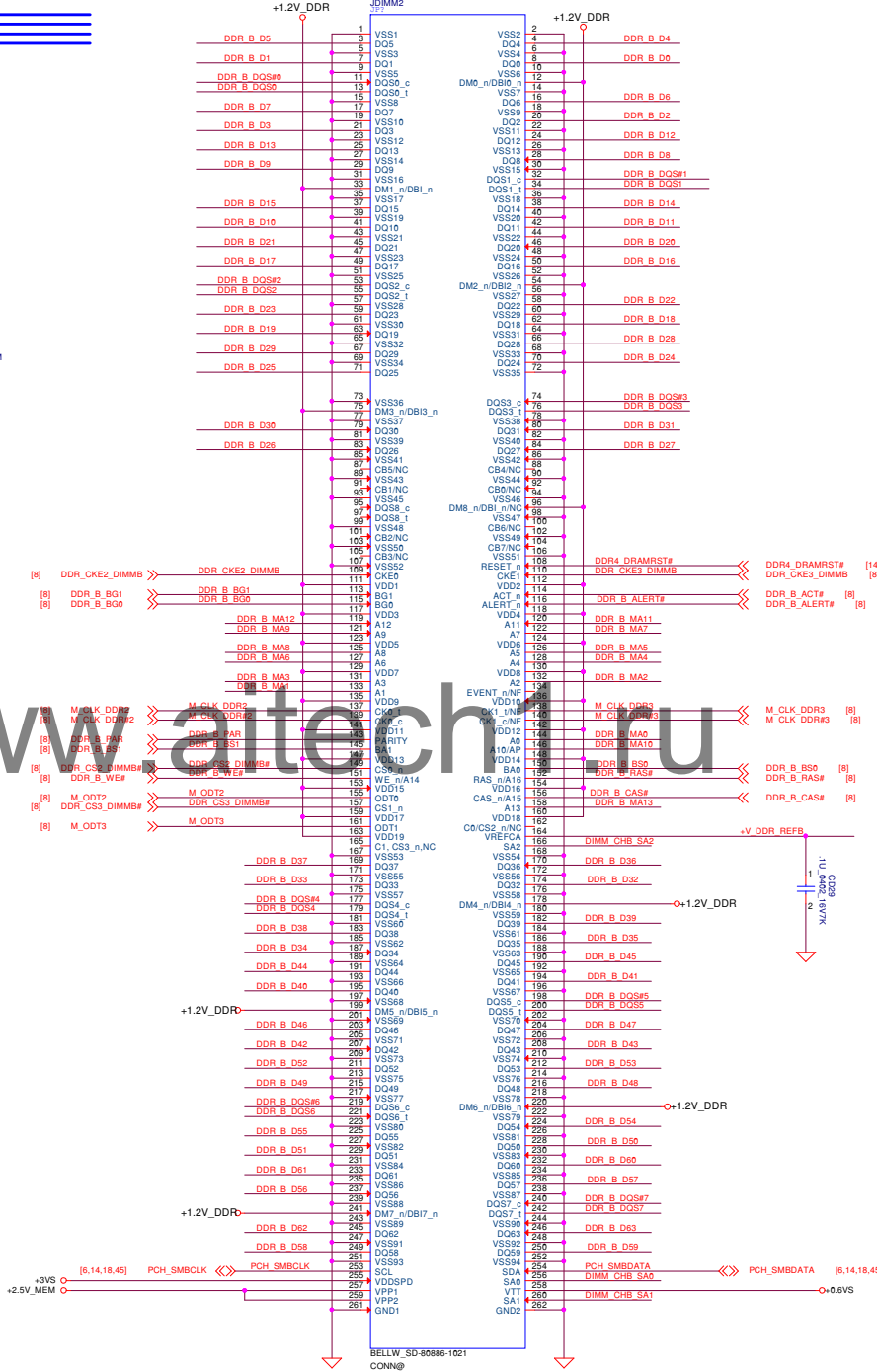
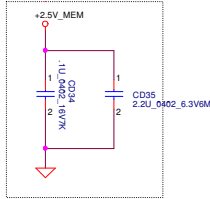
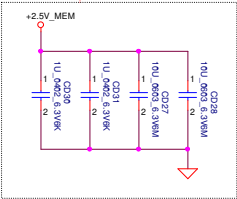
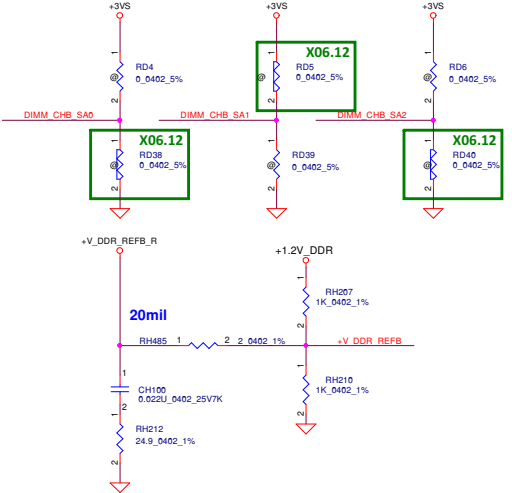
Bottom Plane Components:

- CD90: 1uF, 0.003, 5VWV
- CD91: 1uF, 0.003, 5VWV
- CD92: 1uF, 0.003, 5VWV
- CD93: 1uF, 0.003, 5VWV
- CD94: 1uF, 0.003, 5VWV
- CD95: 1uF, 0.003, 5VWV
- CD96: 1uF, 0.003, 5VWV
- CD97: 1uF, 0.003, 5VWV
- CD98: 1uF, 0.003, 5VWV
- CD99: 1uF, 0.003, 5VWV
- CD100: 1uF, 0.003, 5VWV
- CD101: 1uF, 0.003, 5VWV

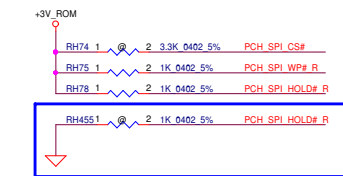
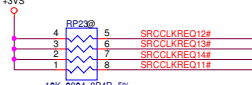
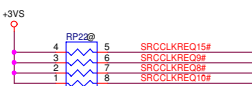
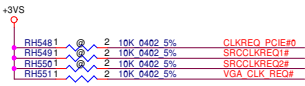
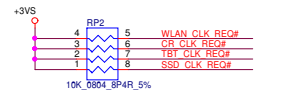
Other Components:

- CD11: 0.1uF, 250V, 0.1uF, 250V, 0.1uF, 250V



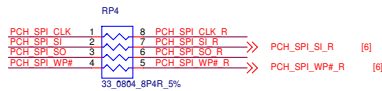


All VREF traces should
have 10 mil trace width

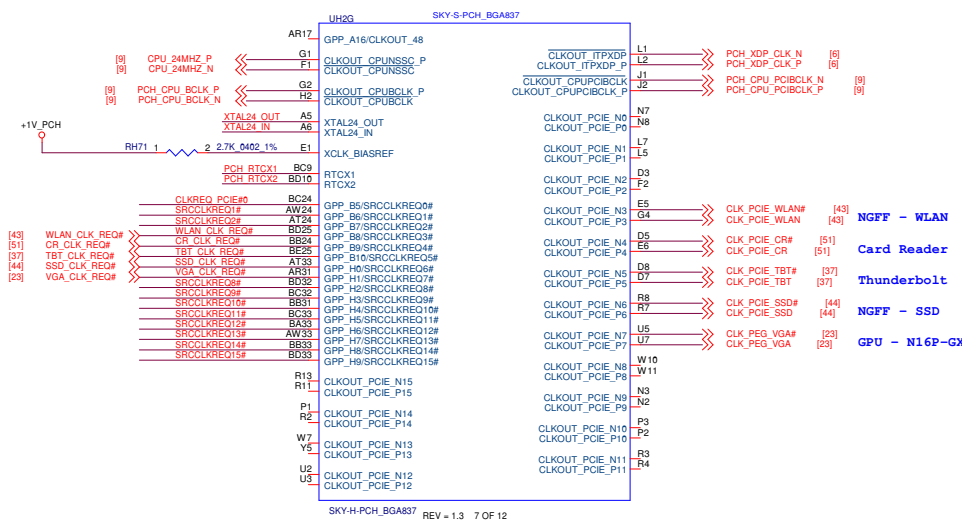


9/5 MOW
Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

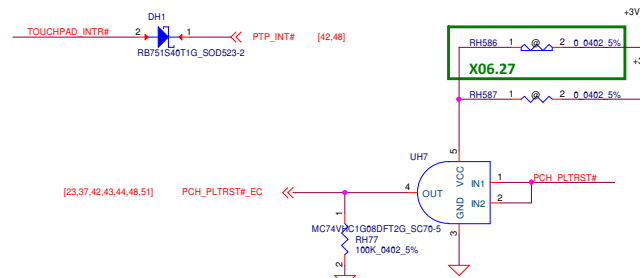
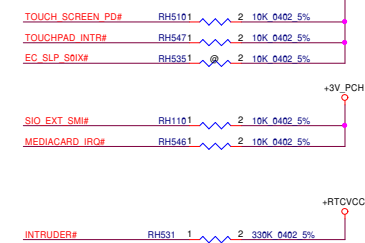
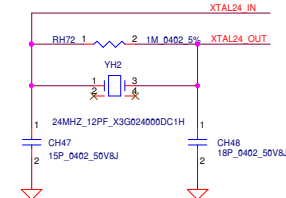
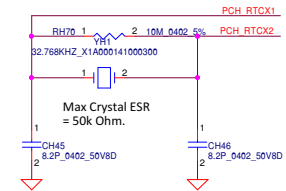
Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-E51/ES1 samples.



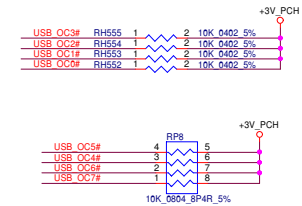
SPI ROM FOR ME (16MByte)



RTC CRYSTAL



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SKY-H-PCH_BGA837 (Left) to **SKY-S-PCH_BGA837** (Right) Pin-to-pin Mapping:

USB Conn 1 (Right Side):

- [47] USB3T1N1 ↔ [47] USB3_1_TXN
- [47] USB3T1P1 ↔ [47] USB3_1_RXN
- [47] USB3N1 ↔ [47] USB3_1_RXP
- [47] USB3R1 ↔ [47] USB3_1_TXN

USB Conn 2 (Left Side):

- [47] USB3T2N1 ↔ [47] USB3_2_TXN
- [47] USB3T2P1 ↔ [47] USB3_2_TXP
- [47] USB3N2 ↔ [47] USB3_2_RXN
- [47] USB3R2 ↔ [47] USB3_2_RXP

SATA:

- [47] SATA_1_TXN ↔ [47] SATA_1_TXN
- [47] SATA_1_RXN ↔ [47] SATA_1_RXN
- [47] SATA_1_RXP ↔ [47] SATA_1_RXP
- [47] SATA_1_TXP ↔ [47] SATA_1_TXP

Other Connections:

- [47] GPP_A1/LAD0/ESPI_I00 ↔ [47] AT22
- [47] GPP_A2/LAD1/ESPI_I01 ↔ [47] A222
- [47] GPP_A3/LAD2/ESPI_I02 ↔ [47] A119
- [47] GPP_A4/LAD3/ESPI_I03 ↔ [47] BD16
- [47] GPP_A5/LFRAME#/ESPI_CS# ↔ [47] BE16
- [47] GPP_A6/SERIO ↔ [47] BA17
- [47] GPP_A7/IRQ#/ESPI_ALERT#0 ↔ [47] AW17
- [47] GPP_A8/RCIN#/ESPI_ALERT#1 ↔ [47] AT17
- [47] GPP_A14/SUS_STATE#/ESPI_RESET# ↔ [47] BC18
- [47] GPP_A9/CLKOUT_LPC0/ESPI_CLK ↔ [47] RH168
- [47] GPP_A10/CLKOUT_LPC1 ↔ [47] RH428
- [47] GPP_G19/SMI# ↔ [47] M45
- [47] GPP_G18/SMI# ↔ [47] N43
- [47] GPP_E6/DEVSLP2 ↔ [47] AE45
- [47] GPP_E5/DEVSLP1 ↔ [47] AG43
- [47] GPP_E4/DEVSLP0 ↔ [47] AG42
- [47] GPP_F6/DEVSLP7 ↔ [47] AB39
- [47] GPP_F8/DEVSLP6 ↔ [47] AB38
- [47] GPP_F7/DEVSLP5 ↔ [47] AB43
- [47] GPP_F6/DEVSLP4 ↔ [47] AB42
- [47] GPP_F5/DEVSLP3 ↔ [47] AB41

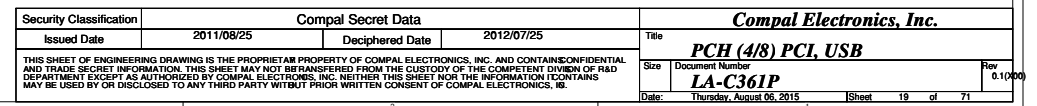
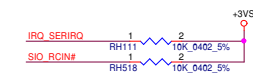
Additional Notes:

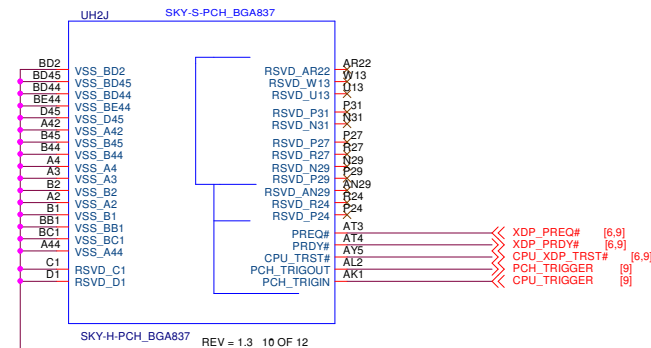
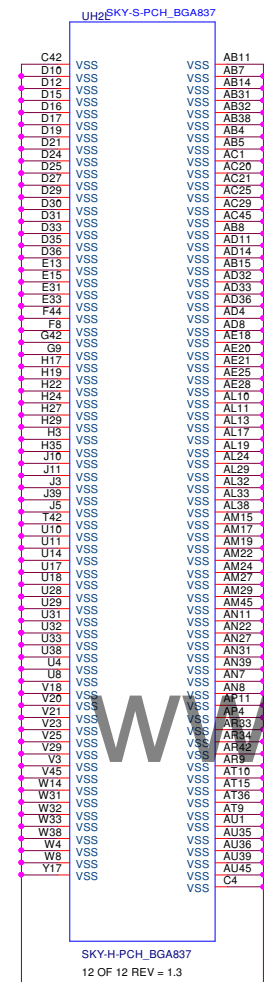
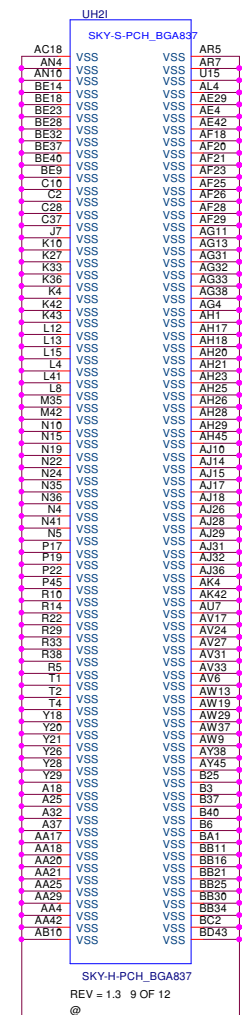
- [48] LPC_AD0 ↔ [48] LPC_AD0
- [48] LPC_AD1 ↔ [48] LPC_AD1
- [48] LPC_AD2 ↔ [48] LPC_AD2
- [48] LPC_AD3 ↔ [48] LPC_AD3
- [48] LPC_FRAME# ↔ [48] LPC_FRAME#
- [48] IRQ_SERIO ↔ [48] IRQ_SERIO
- [45] FFS_INT1 ↔ [45] FFS_INT1
- [45] SIO_RCIN# ↔ [45] SIO_RCIN#
- [48] CLK_PCI_MEC ↔ [48] CLK_PCI_MEC
- [48] PCI_CLK_LPC1 ↔ [48] PCI_CLK_LPC1
- [44] mSATA_DEVSPL ↔ [44] mSATA_DEVSPL

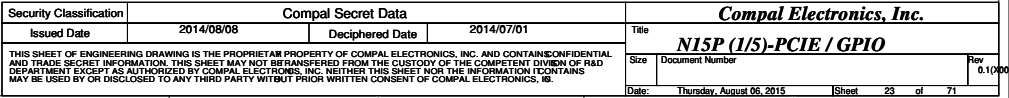
SKY-H-PCH_BGA837 (Left) to **SKY-S-PCH_BGA837** (Right) Pin-to-pin Mapping

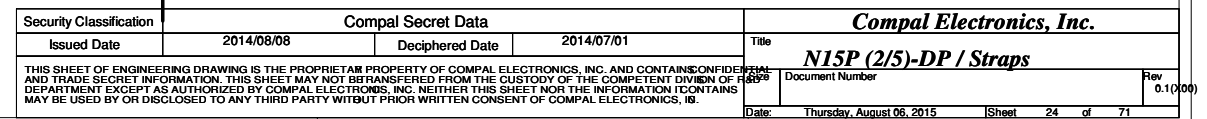
REV = 1.3 6 OF 12

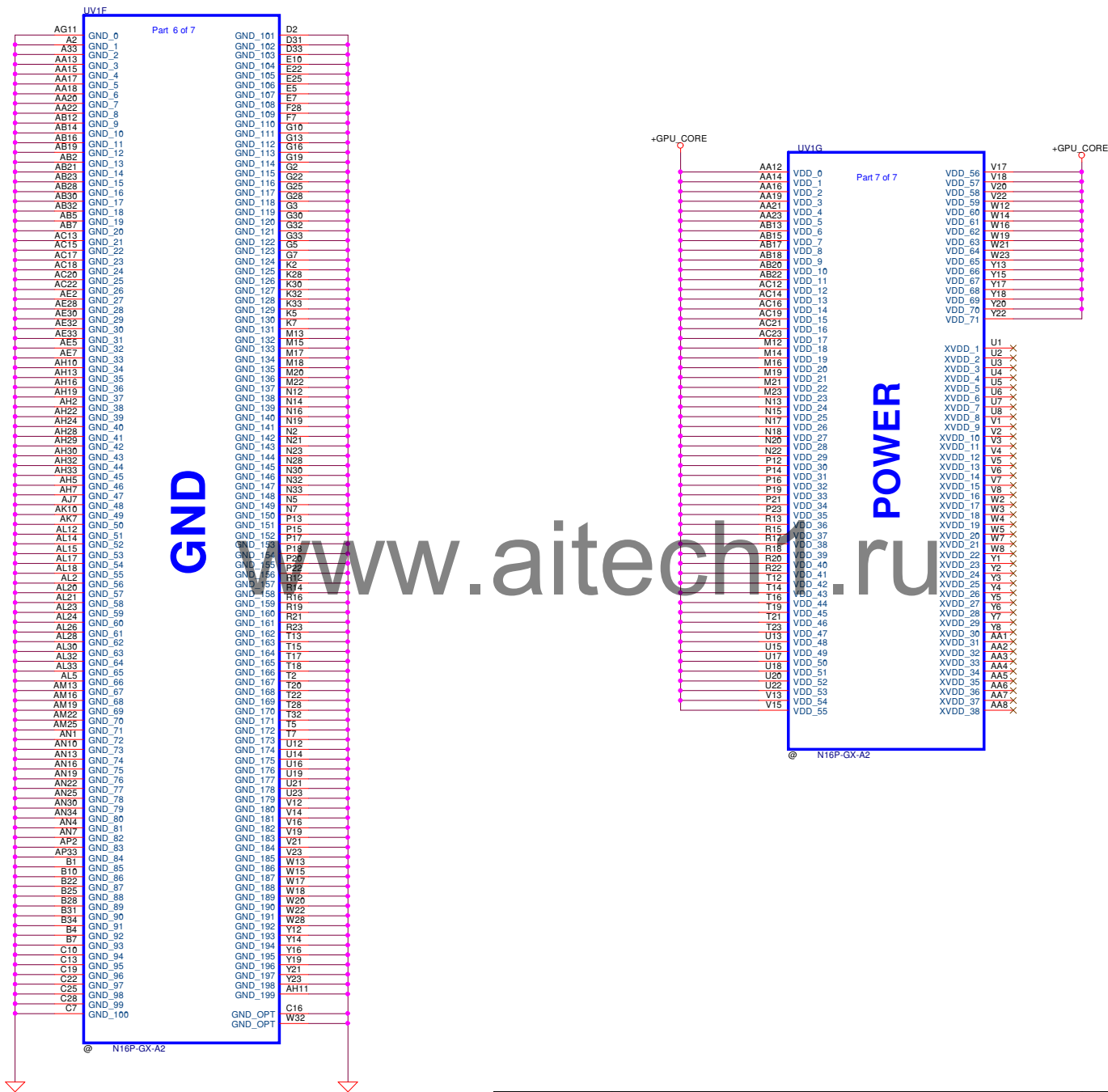
PCI_CLK_LPC1



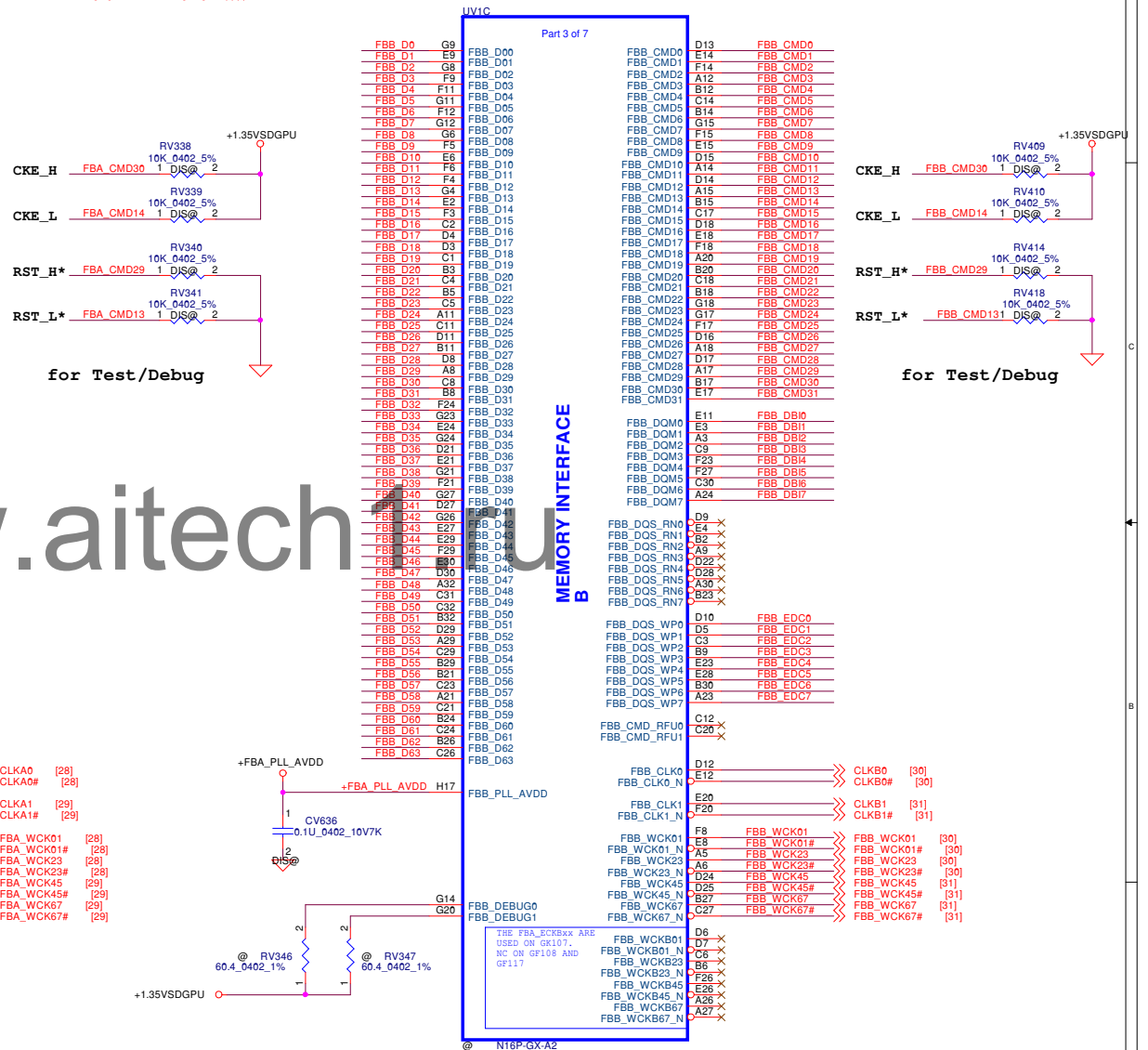
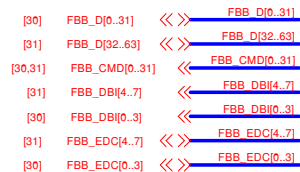








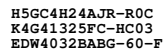
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/08/08	Deciphered Date	2014/07/01	Title	N15P (4/5)-Power / GND
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64X32 GDDR5

G82-64, G84-128	Channel 0 0..31	G82-64, G84-128	Channel 1 32..63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A8_A11	CMD23	A8_A11
CMD8	AB*	CMD24	AB*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	RS1*	CMD29	RS1*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

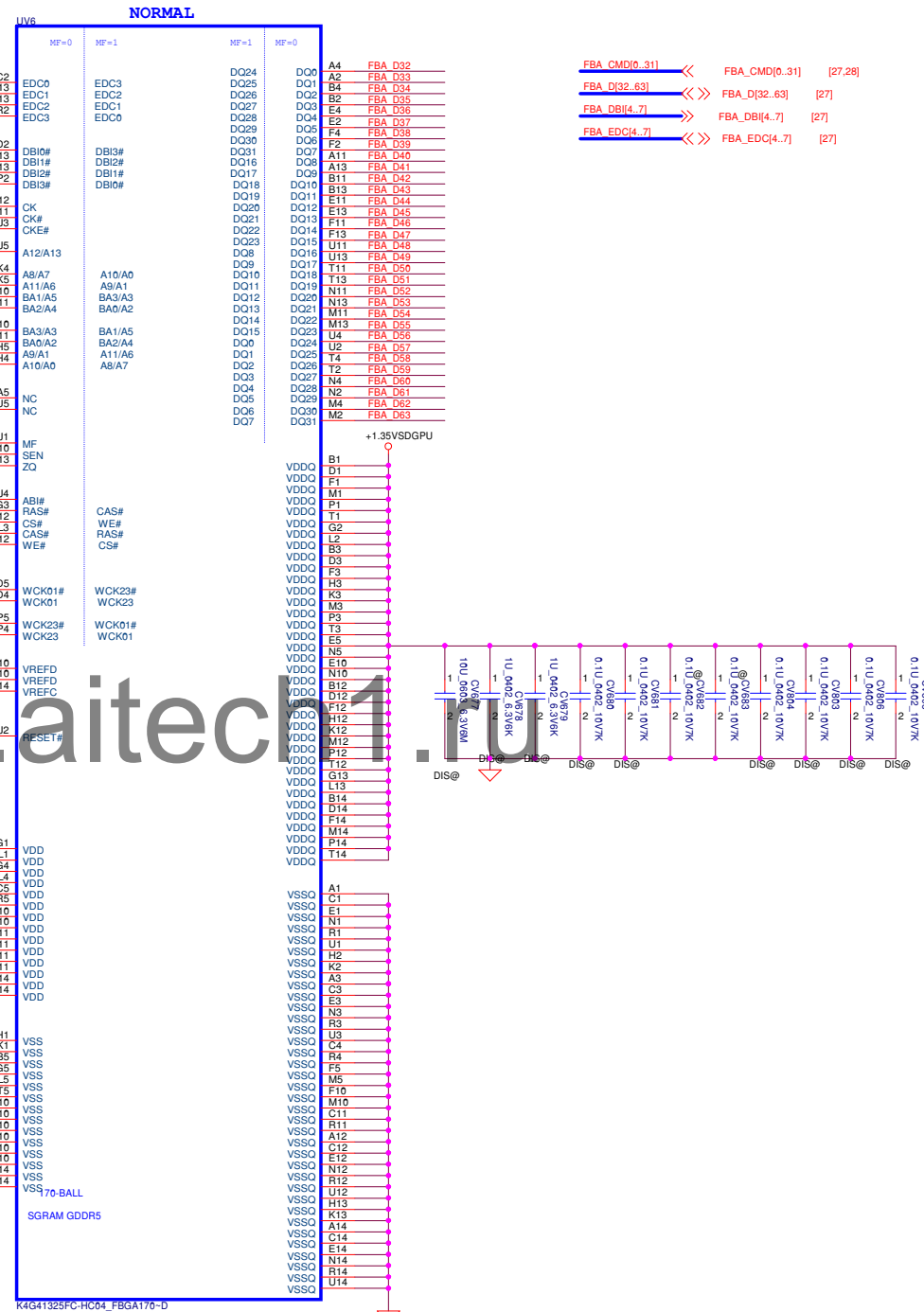
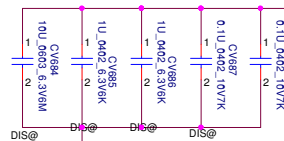
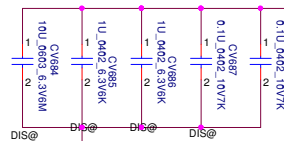
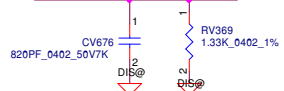
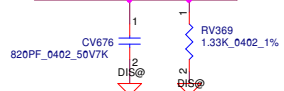
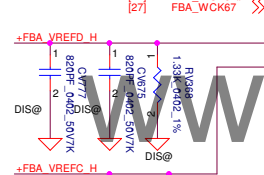
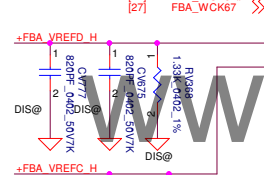
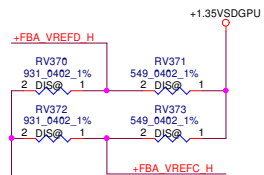
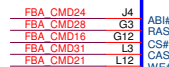
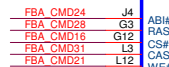
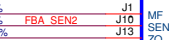
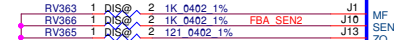
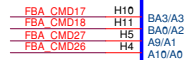
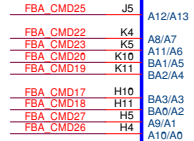
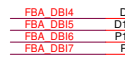
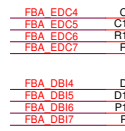
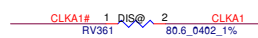


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Memory Partition A - Upper 32 bits

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A8_A11	CMD23	A8_A11
CMD8	AB*	CMD24	AB*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	R5*	CMD29	R5*
CMD14	CR*	CMD30	CR*
CMD15	CAS*	CMD31	CAS*



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Compal Electronics, Inc.		
Title VRAM GDDR5 A Upper		
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64X32 GDDR5

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	C5*	CMD16	C3*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CNE*	CMD30	CNE*
CMD15	CAS*	CMD31	CAS*



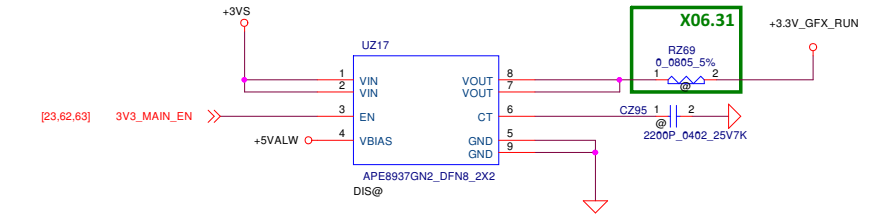
Security Classification		Compal Secret Data		Compal Electronics, Inc. VRAM GDDR5 B Lower	
Issued Date	2014/08/08	Deciphered Date	2014/07/01	Title	VRAM GDDR5 B Lower Document Number Date: Thursday, August 06, 2015 Sheet 30 of 71
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					0.1(00)

Memory Partition B - Upper 32 bits

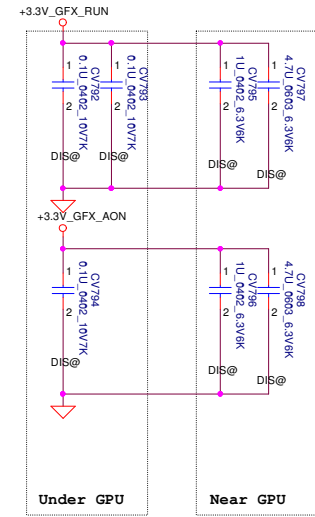
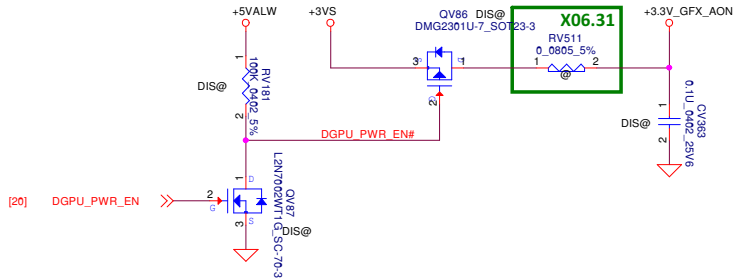
Table 46. GDDR5 Mode H Mapping

GDDR4+ Channel 0 0-31	GDDR4+ Channel 1 32-63	GDDR4+ Channel 2 64-95	GDDR4+ Channel 3 96-127
CM00	CM04	CM08	CM12
CM01	CM05	CM09	CM13
CM02	CM06	CM10	CM14
CM03	CM07	CM11	CM15
CM04	CM08	CM12	CM16
CM05	CM09	CM13	CM17
CM06	CM10	CM14	CM18
CM07	CM11	CM15	CM19
CM08	CM12	CM16	CM20
CM09	CM13	CM17	CM21
CM10	CM14	CM18	CM22
CM11	CM15	CM19	CM23
CM12	CM16	CM20	CM24
CM13	CM17	CM21	CM25
CM14	CM18	CM22	CM26
CM15	CM19	CM23	CM27
CM16	CM20	CM24	CM28
CM17	CM21	CM25	CM29
CM18	CM22	CM26	CM30
CM19	CM23	CM27	CM31
CM20	CM24	CM28	CM32
CM21	CM25	CM29	CM33
CM22	CM26	CM30	CM34
CM23	CM27	CM31	CM35
CM24	CM28	CM32	CM36
CM25	CM29	CM33	CM37
CM26	CM30	CM34	CM38
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CM28	CM32	CM36	CM40
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CM41	CM45	CM49	CM53
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CM43	CM47	CM51	CM55
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CM45	CM49	CM53	CM57
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CM58	CM62	CM66	CM70
CM59	CM63	CM67	CM71
CM60	CM64	CM68	CM72
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CM64	CM68	CM72	CM76
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CM258	CM262	CM266	CM270
CM259	CM263	CM267	CM271
CM260	CM264	CM268	CM272
CM261	CM265	CM269	CM273
CM262	CM266	CM270	CM274
CM263	CM267	CM271	CM275
CM264	CM268	CM272	CM276
CM265	CM269	CM273	CM277
CM266	CM270	CM274	CM278
CM267	CM271	CM275	CM279
CM268	CM272	CM276	CM280
CM269	CM273	CM277	CM281
CM270	CM274	CM278	CM282
CM271	CM275	CM279	CM283
CM272	CM276	CM280	CM284
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CM274	CM278	CM282	CM286
CM275	CM279	CM283	CM287
CM276	CM280	CM284	CM288
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CM310	CM314	CM318	CM322
CM311	CM315	CM319	CM323
CM312	CM316	CM320	CM324
CM313	CM317	CM321	CM325
CM314	CM318	CM322	CM326
CM3			

+3.3V_GFX_RUN



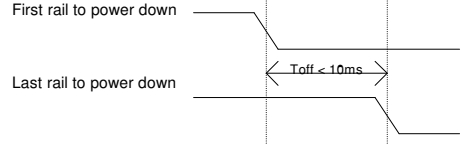
+3VALW to +3.3V_GFX_AON



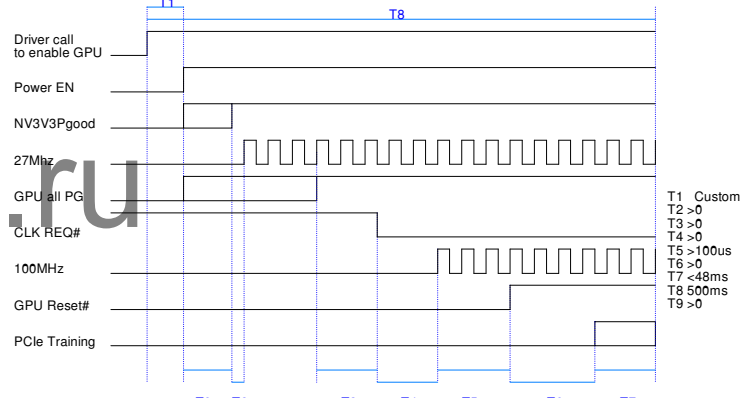
GPU Power Up Power Rail Sequence



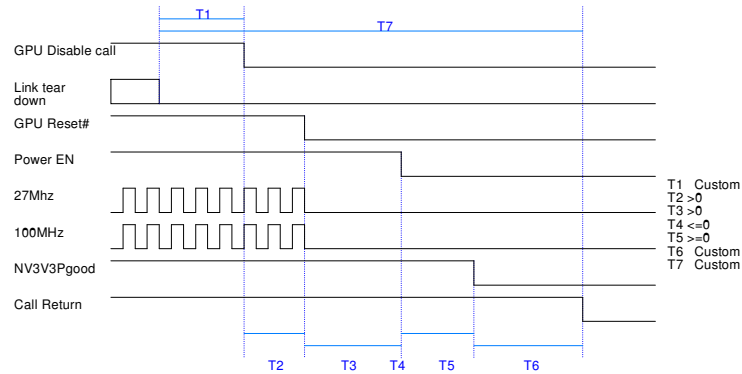
GPU Power Down Sequence



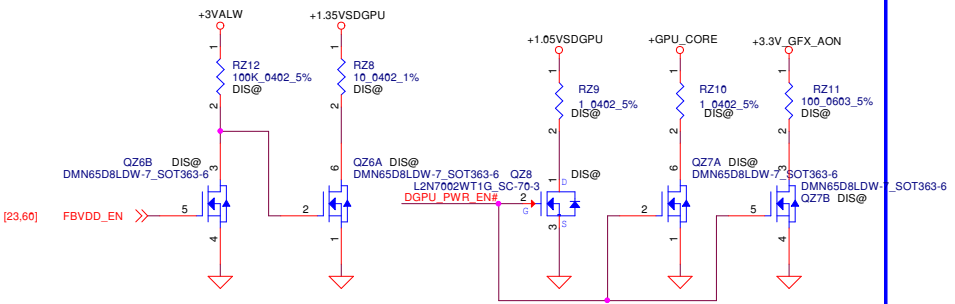
GPU Power Up Sub-system Sequence



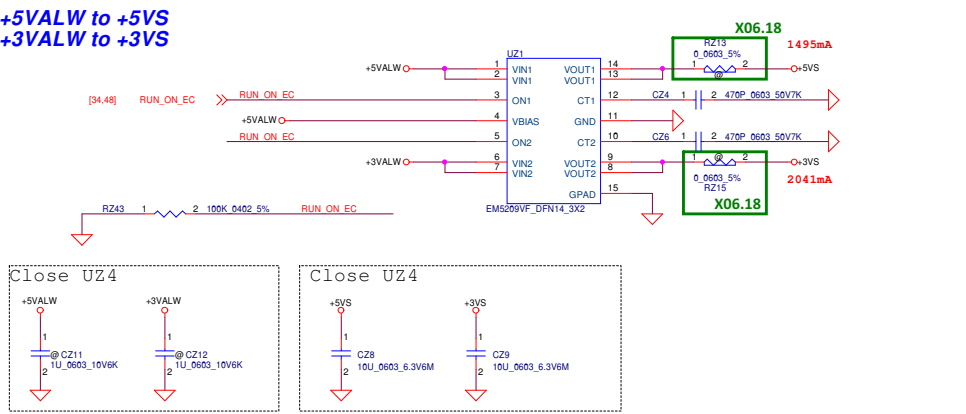
GPU Power Down Sub-system Sequence



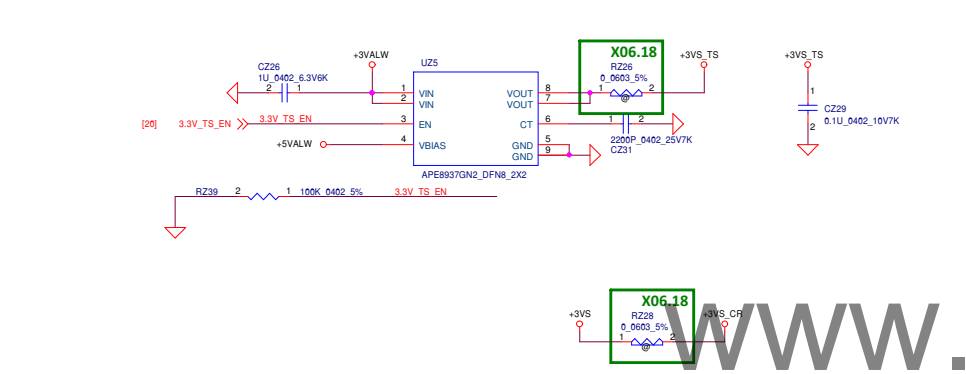
Discharge



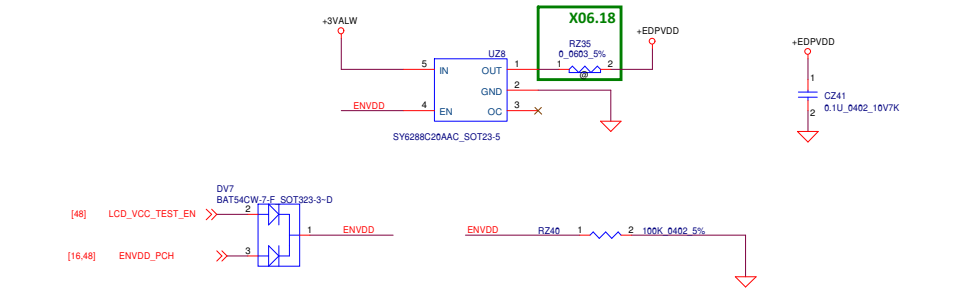
+5VALW to +5VS
+3VALW to +3VS



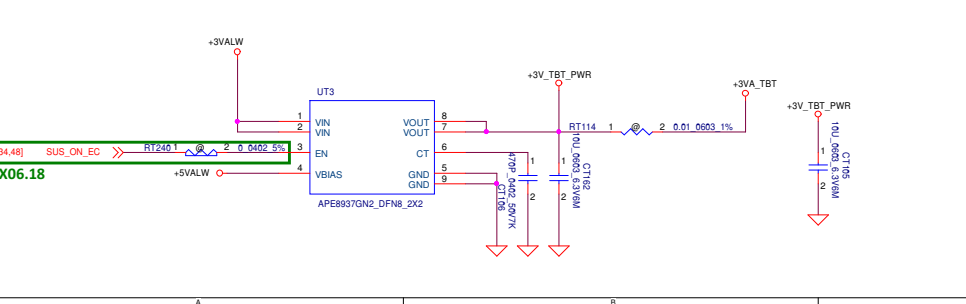
Touch Screen Load Switch & Card Reader



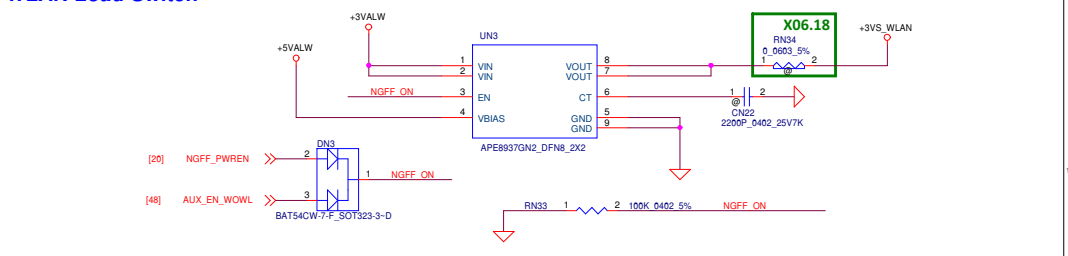
eDP & Camera Load Switch



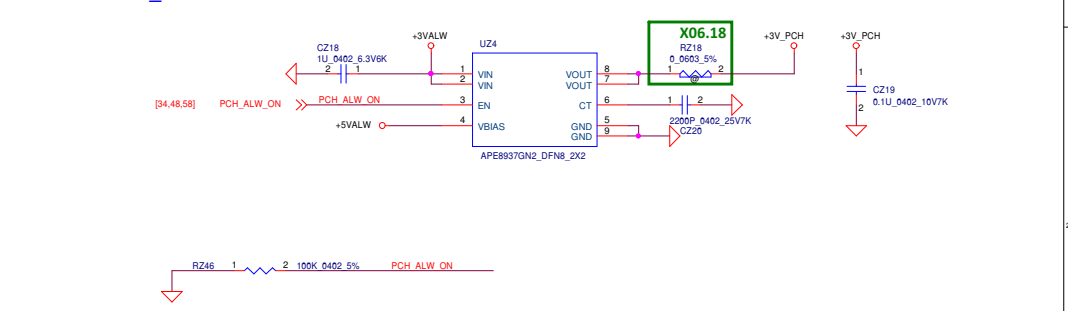
Alpine Ridge(TBT) Load Switch



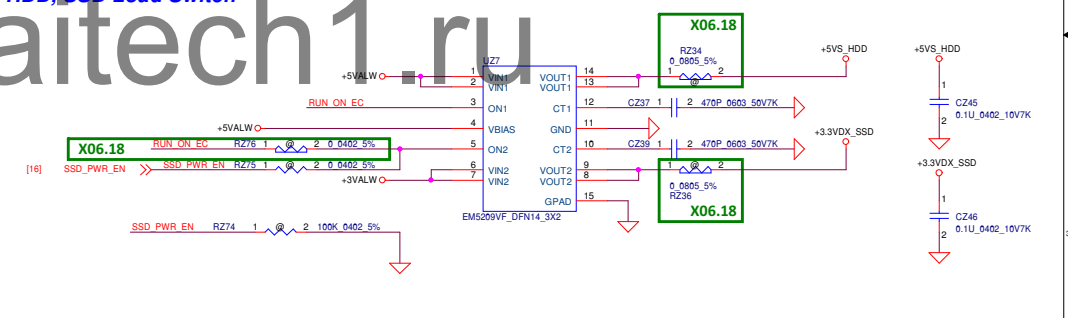
WLAN Load Switch



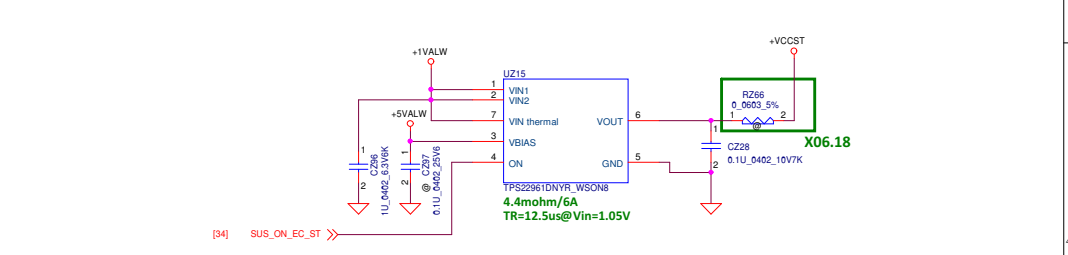
+3VALW to +3V_PCH



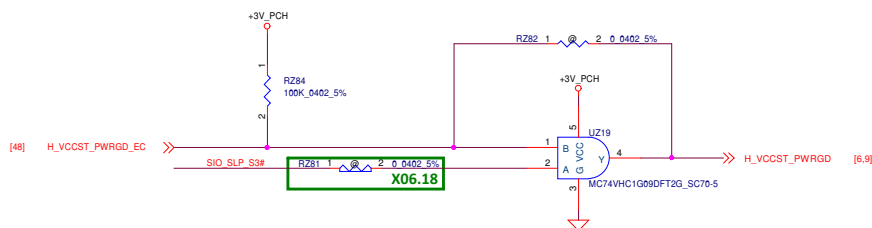
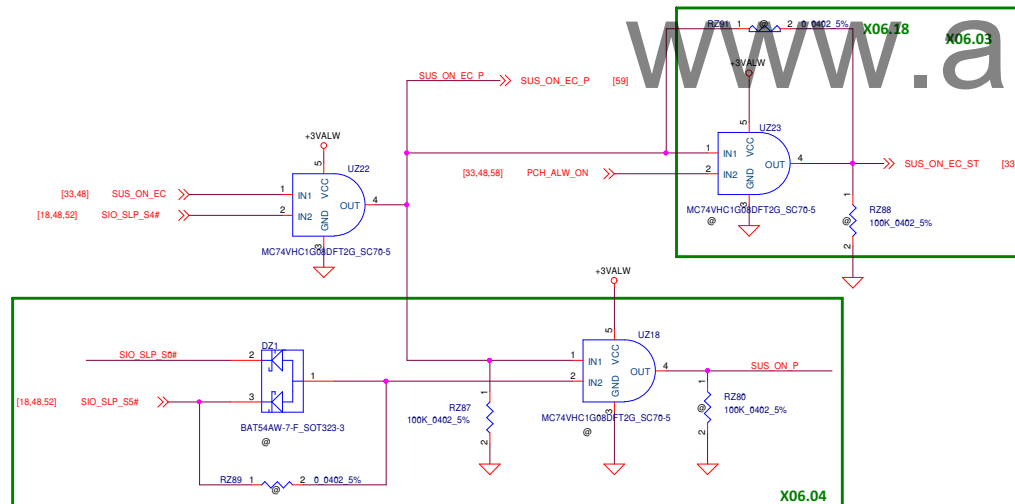
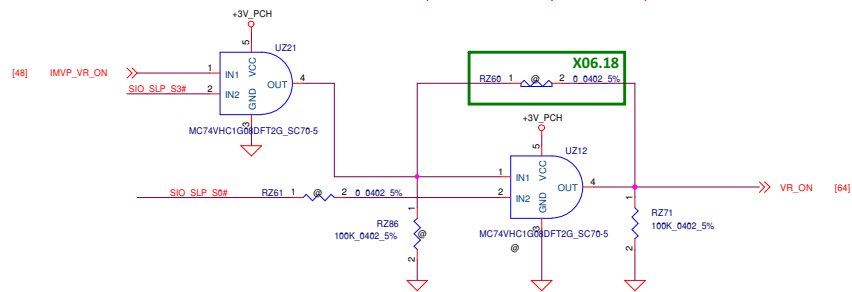
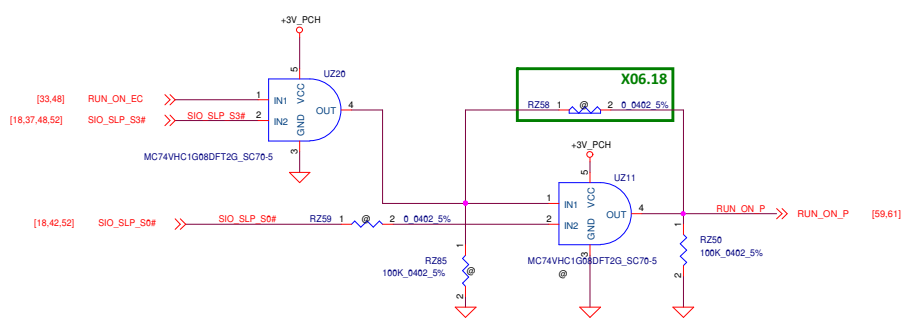
HDD,SSD Load Switch



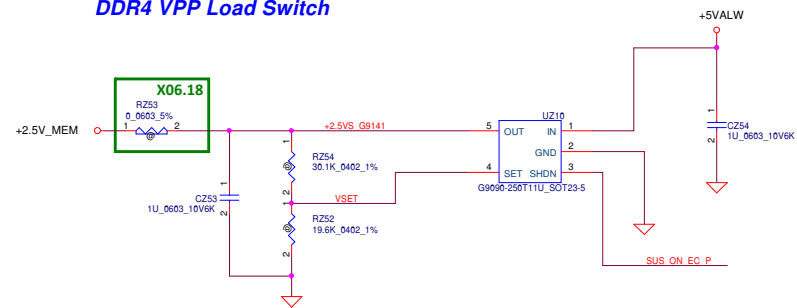
+VCCST Load Switch



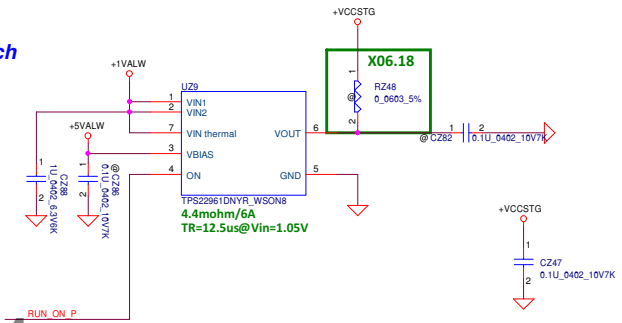
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				Size
				Document Number
				LA-C361P
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				0.1(000)
				Date
				Thursday, August 06, 2015
				Sheet
				33 of 71



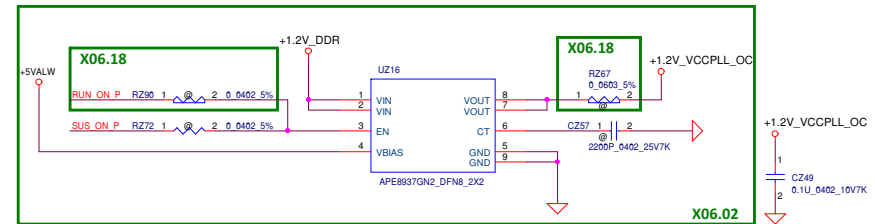
DDR4 VPP Load Switch



+VCCSTG Load Switch

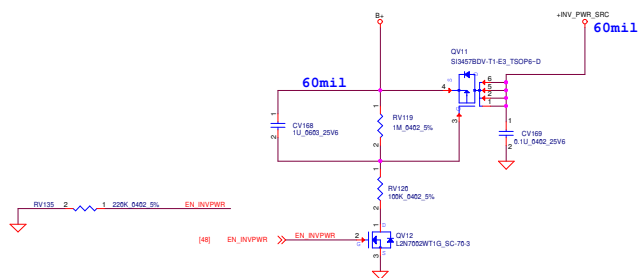


+VCCPLL_OC Load Switch

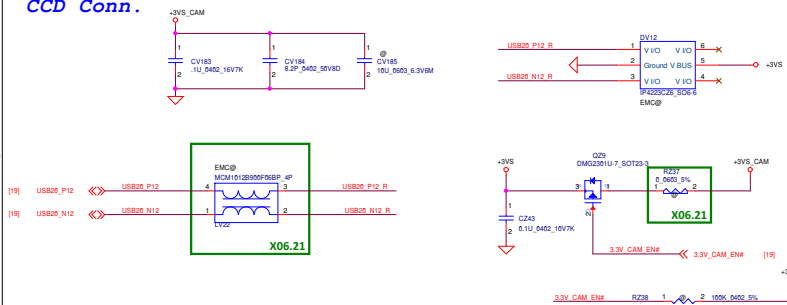


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				Size	Document Number
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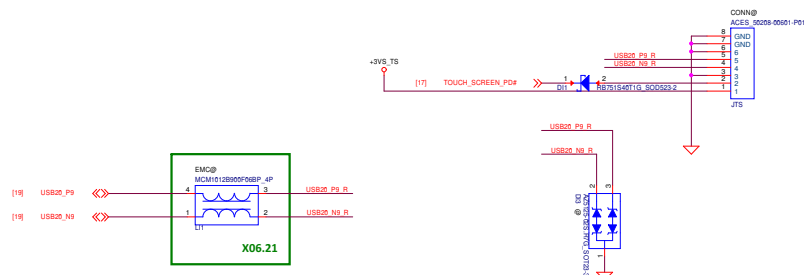
LCD backlight PWR CTRL



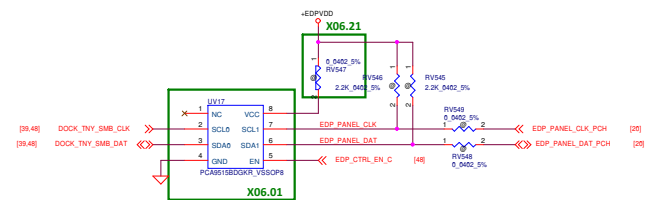
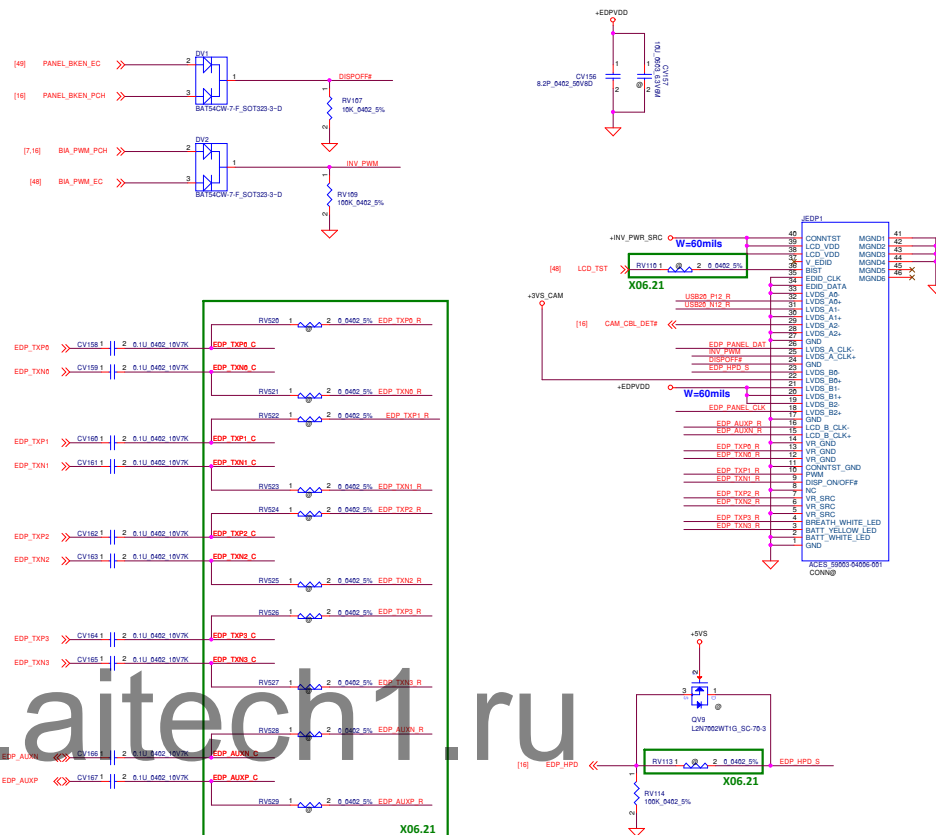
CCD Conn.



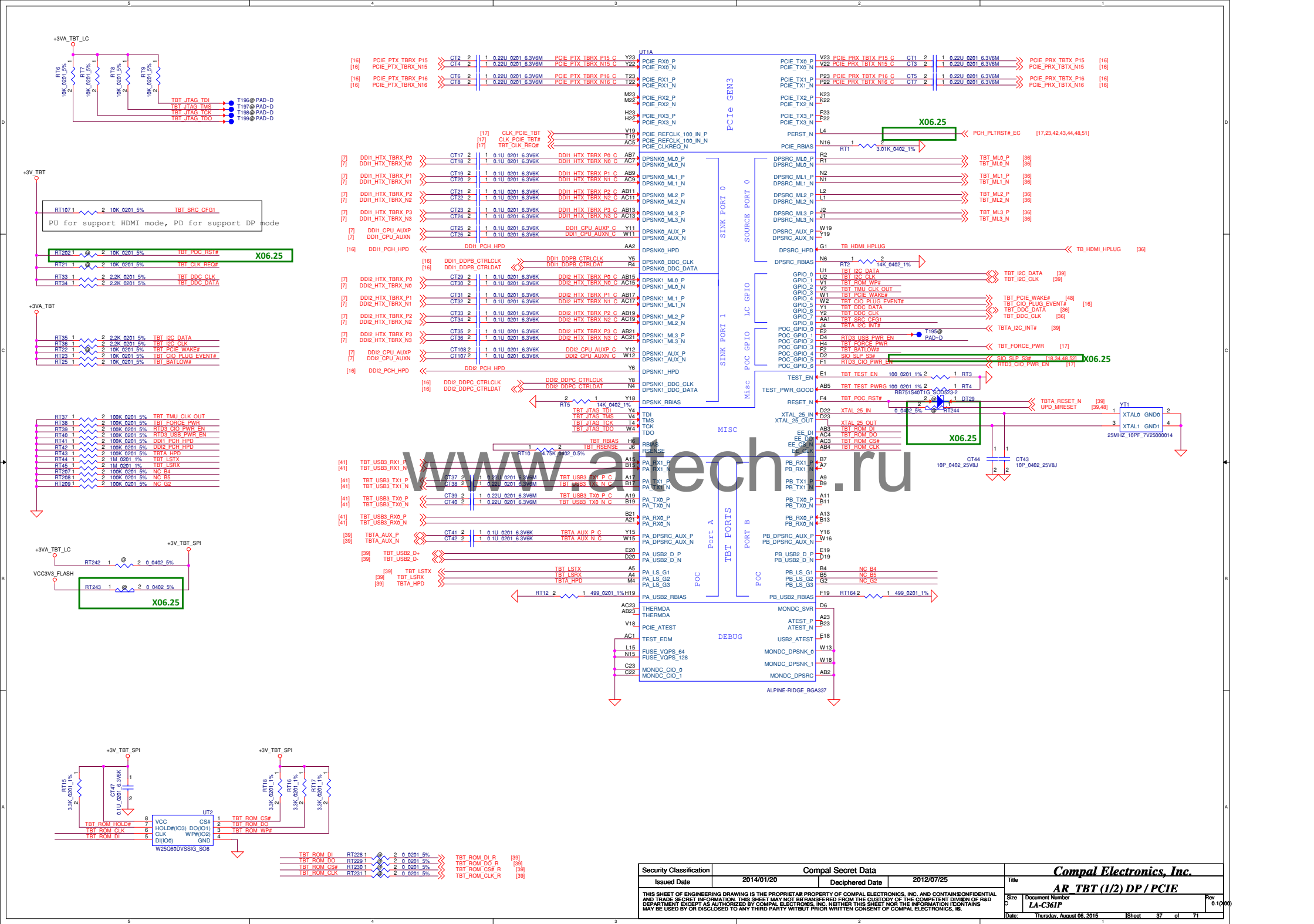
Touch Screen Conn.



eDP & TS Conn.



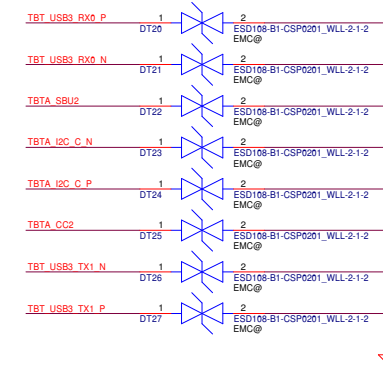
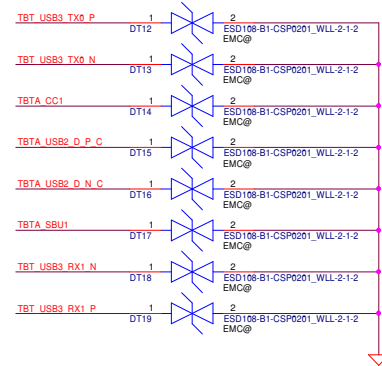
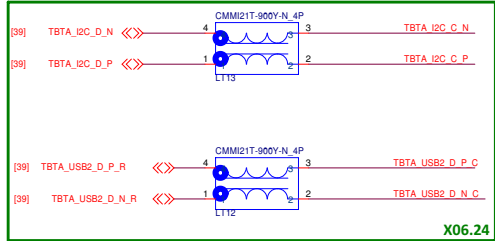
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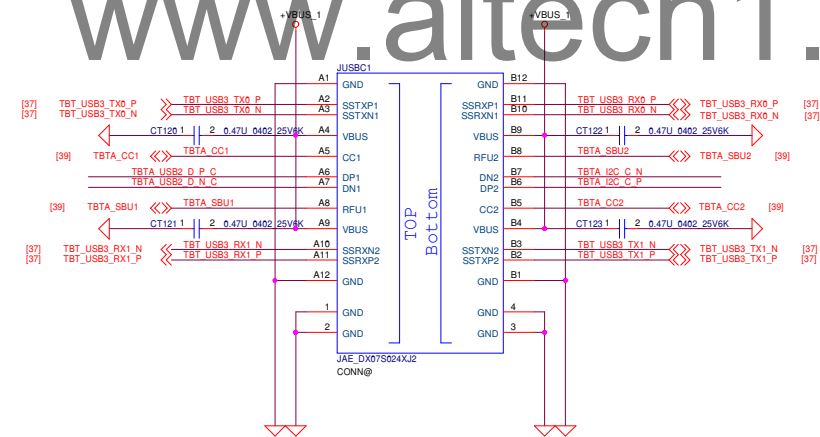
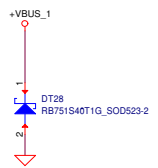
Reserve

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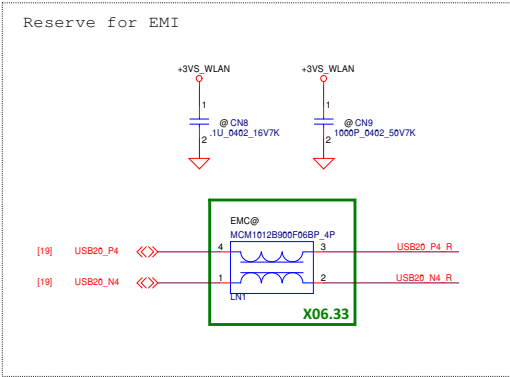
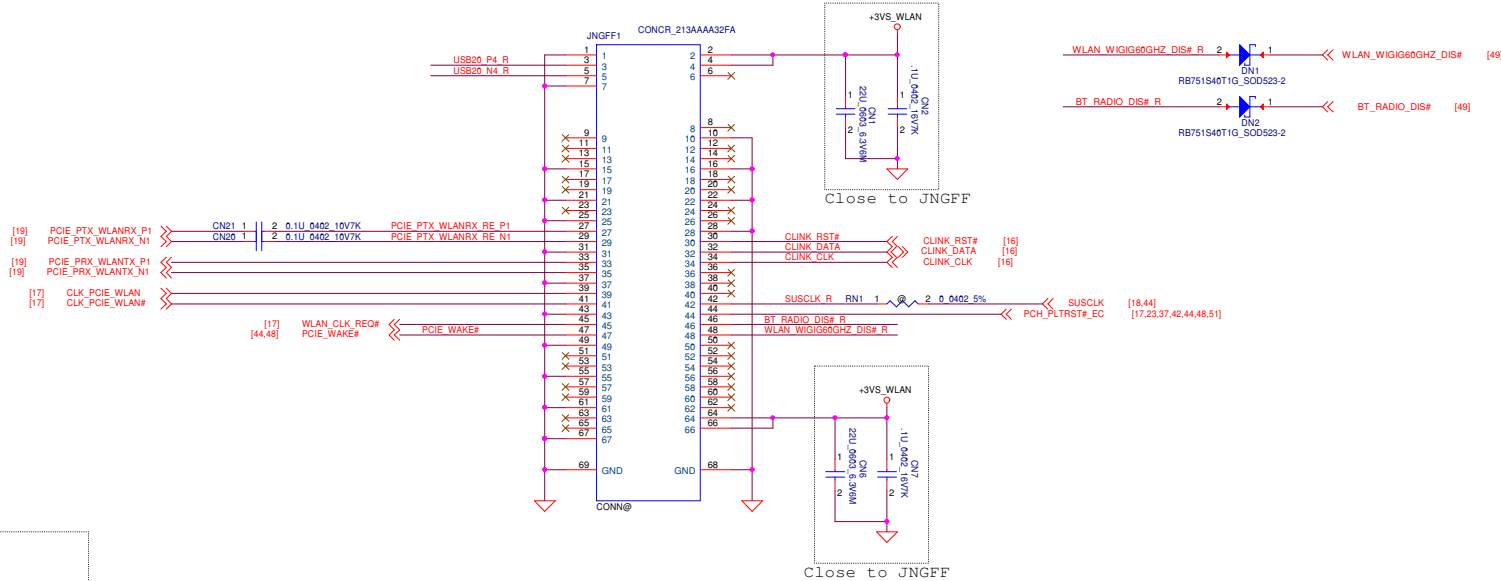


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M.2 Slot-A Key-A (WLAN + BT)

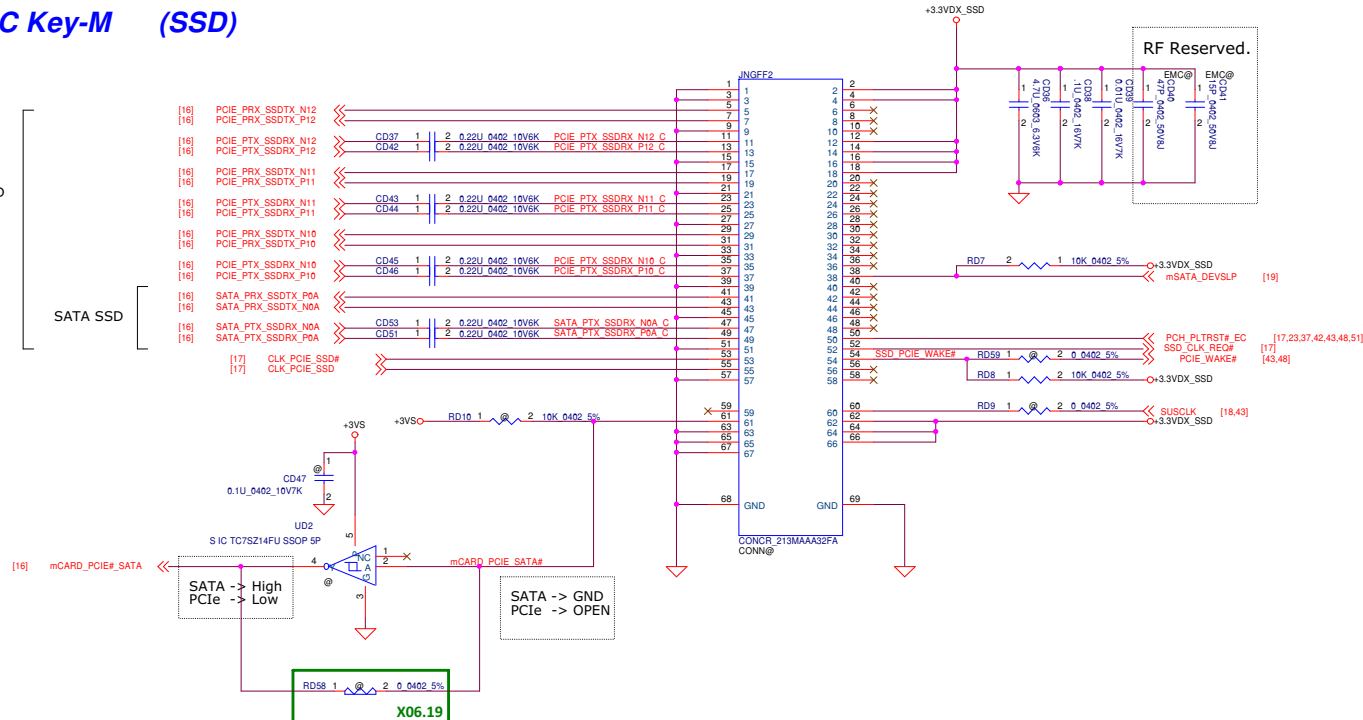


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M.2 Slot-C Key-M (SSD)

PCIe SSD

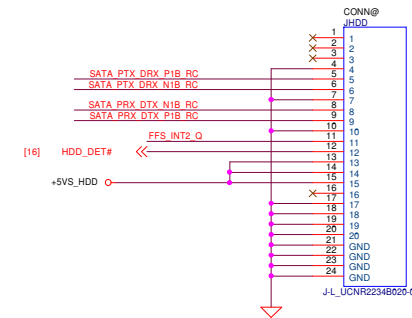
SATA SSD



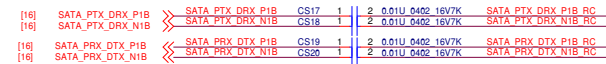
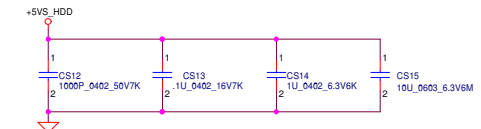
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HDD CONN

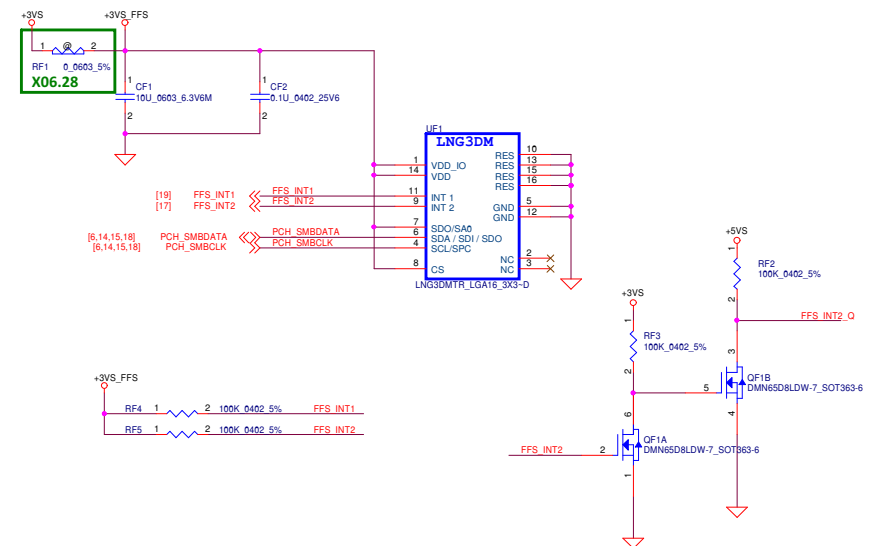


Place near HDD CONN (JHDD1)



BYPASS Circuit

Free Fall Sensor

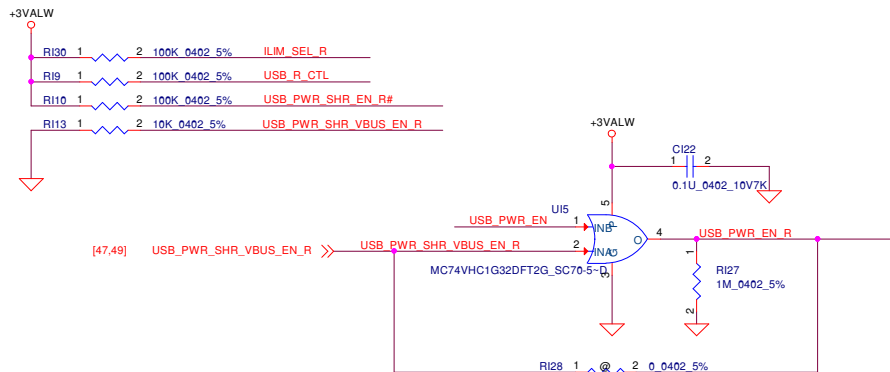


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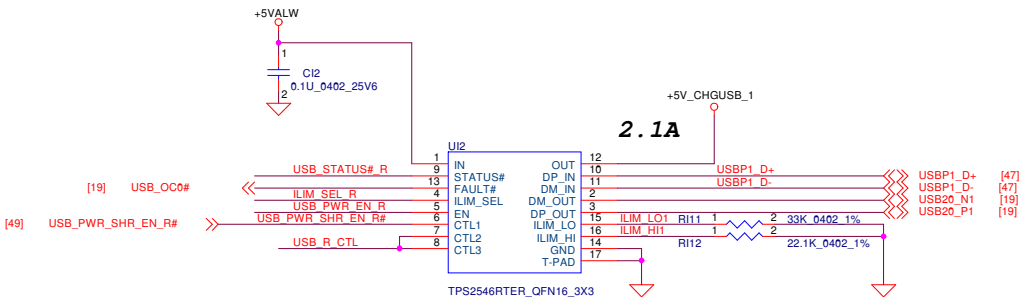
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (ForSupport USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI=2.2A)

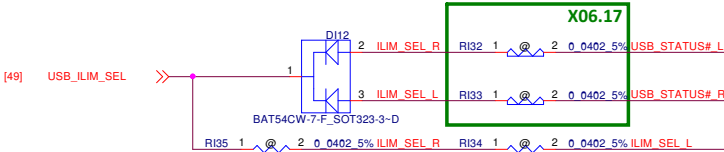
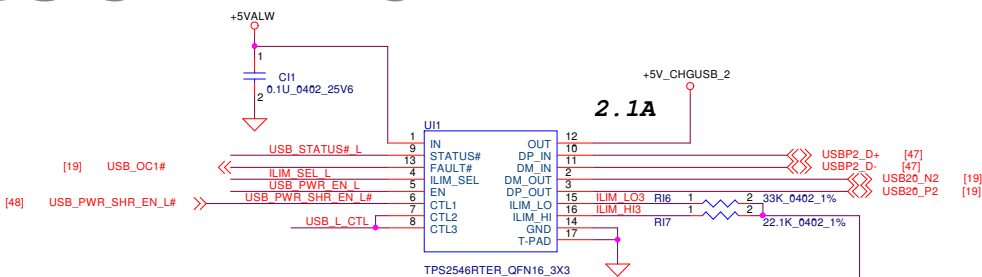
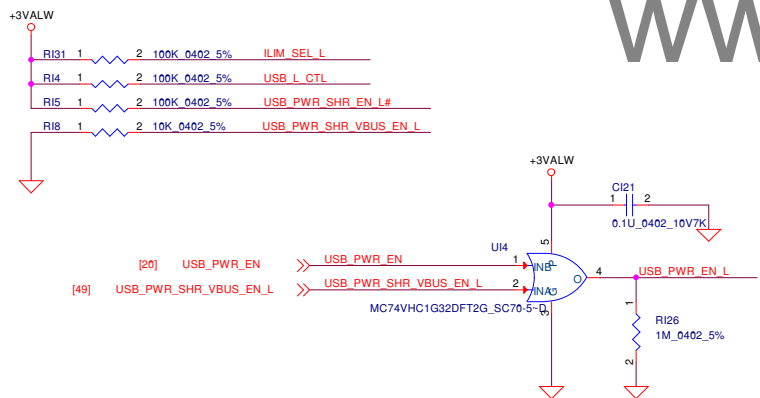


USB3.0 / USB2.0 Port1 (Right Side)

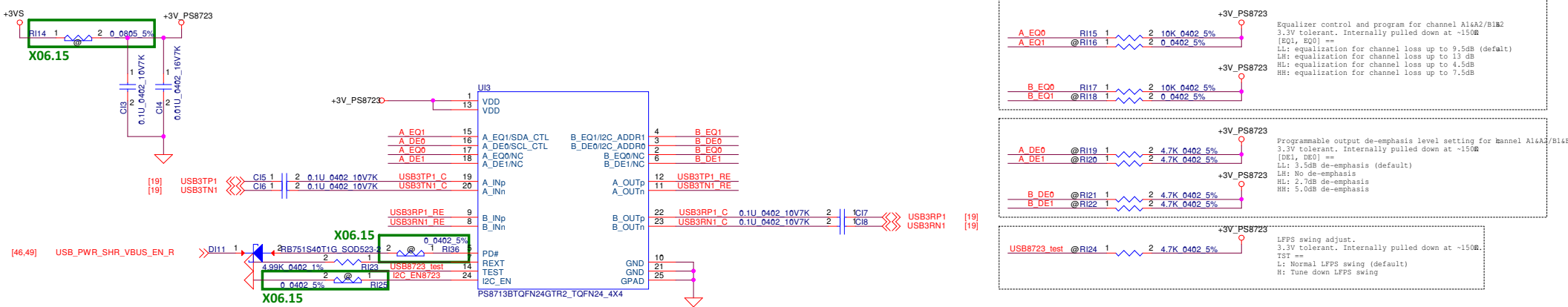


USB3.0 / USB2.0 Port2 (Left Side)

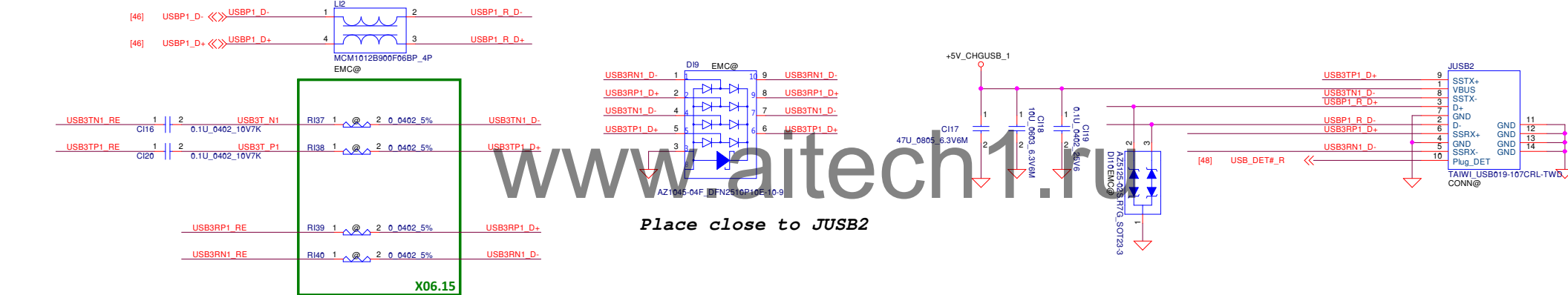
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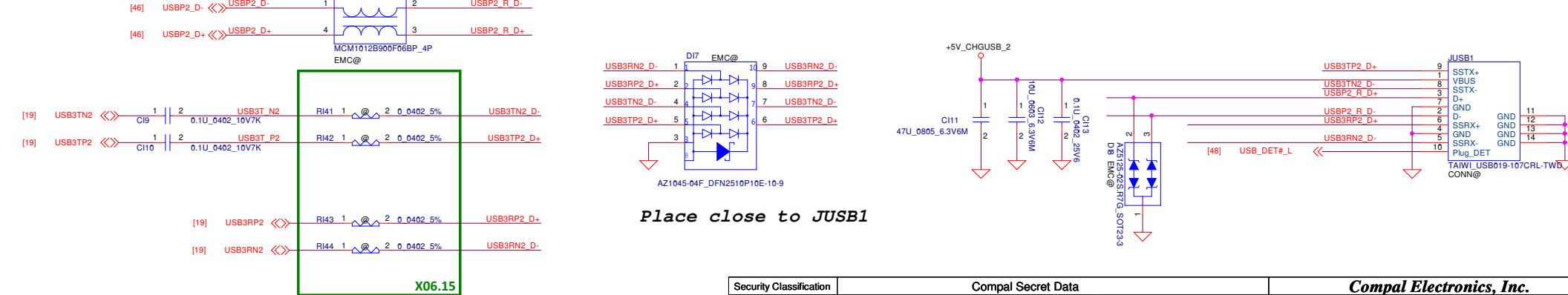
USB3.0 Re-driver

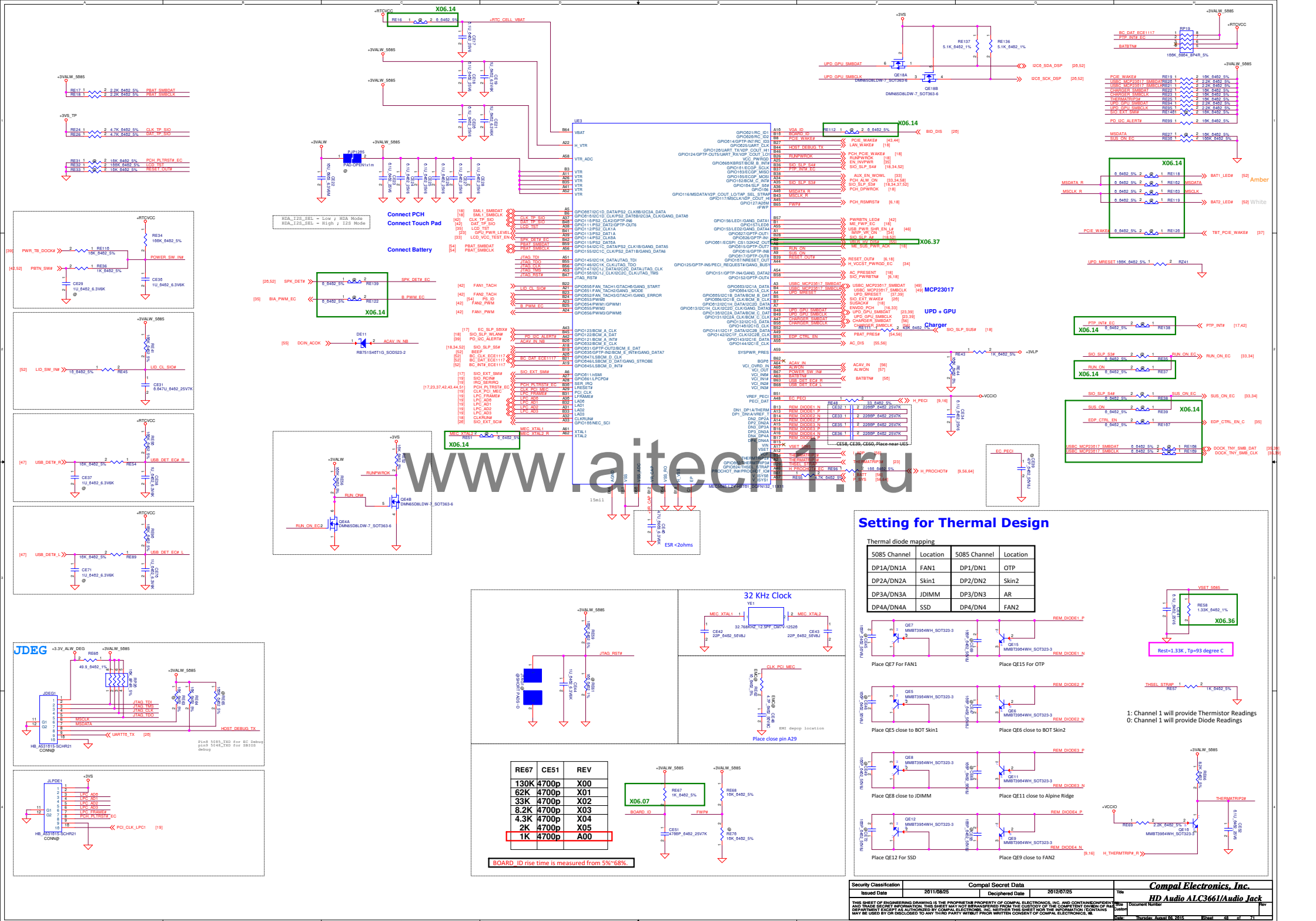


USB3.0 / USB2.0 Port1 (Right Side)

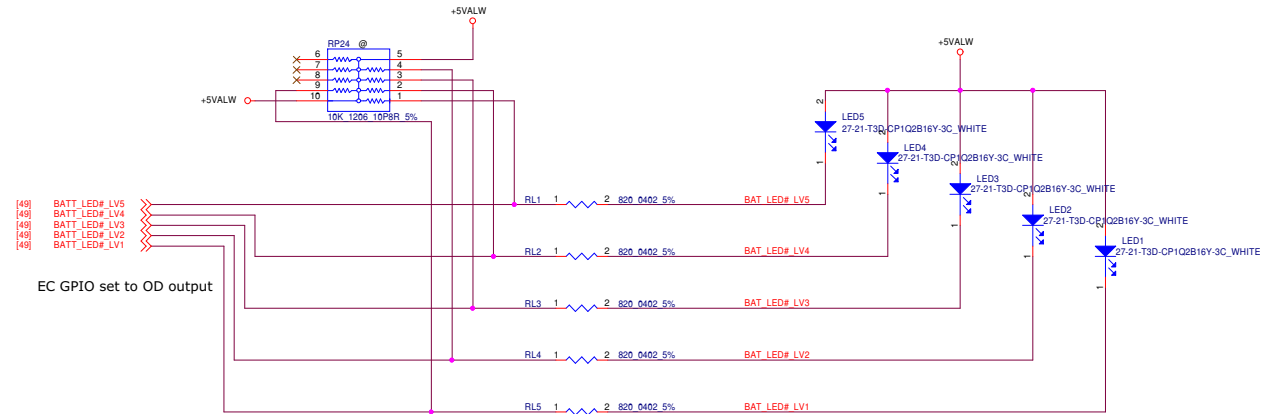
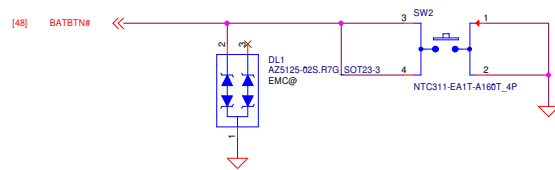


USB3.0 / USB2.0 Port2 (Left Side)





Battery Gauge LED

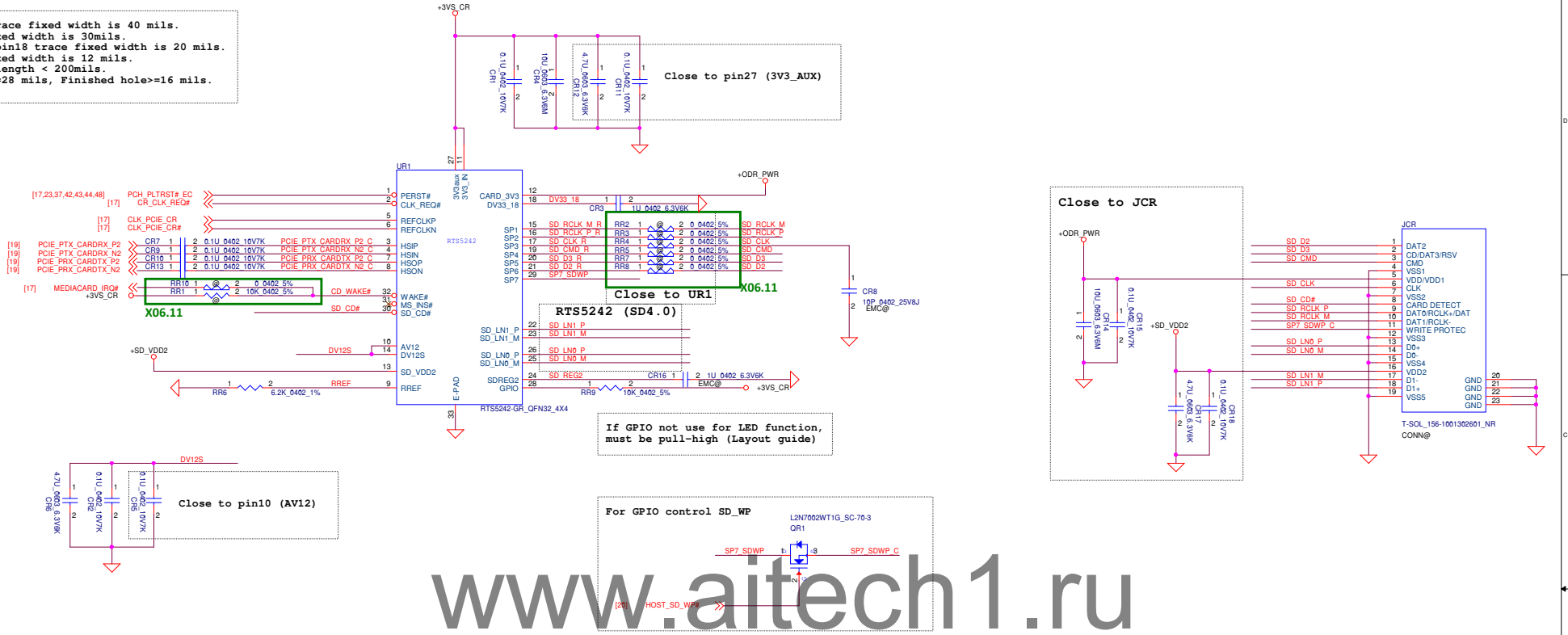


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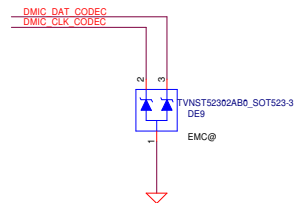
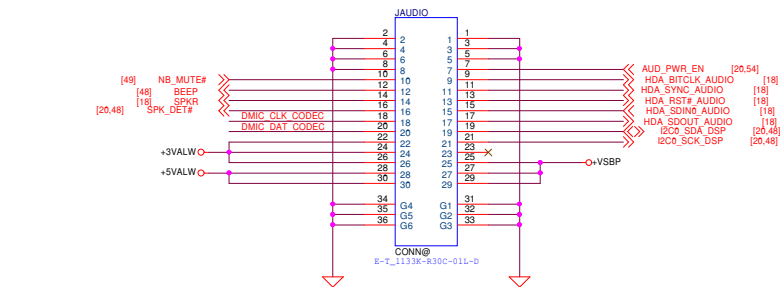
Card Reader

Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=28 mils, Finished hole>=16 mils.

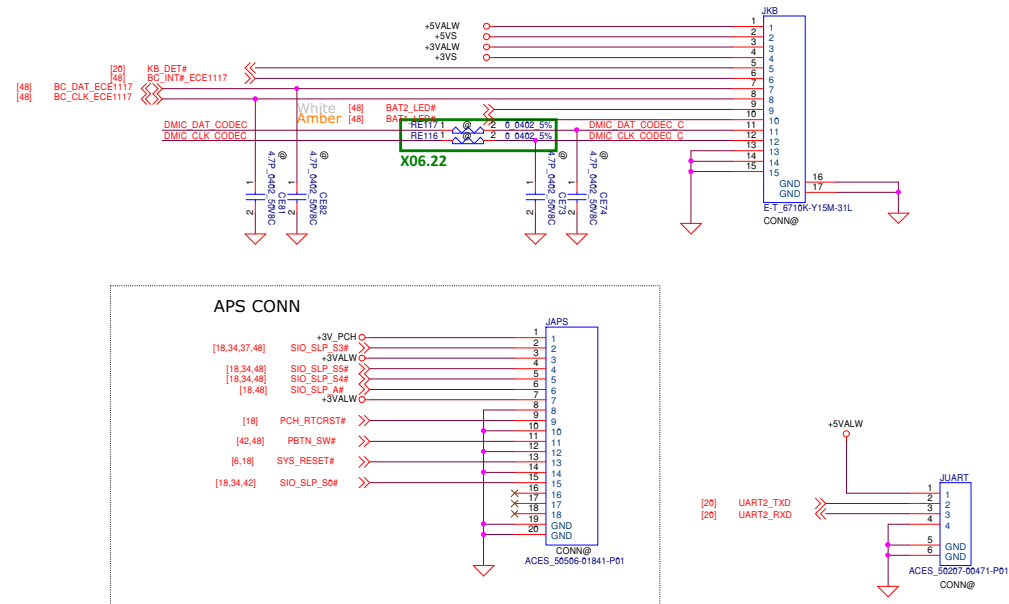


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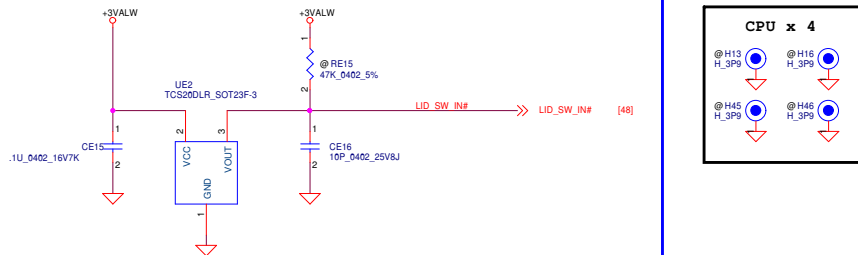
AUDIO Board Conn.



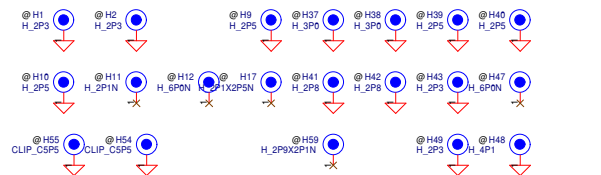
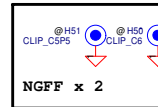
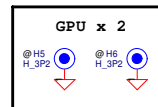
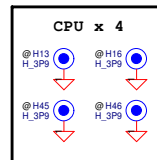
Keyboard Controller board + DMIC



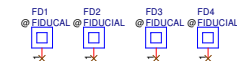
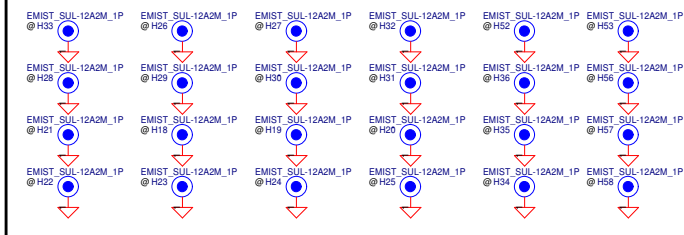
Lid Switch



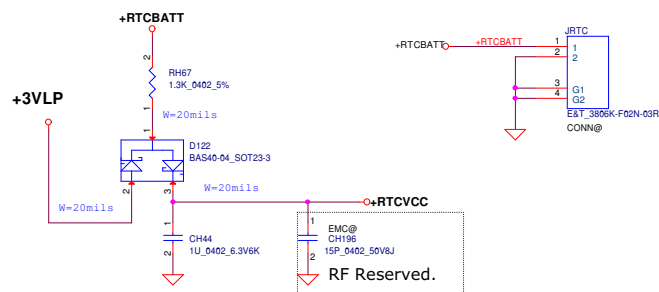
Screw Hole



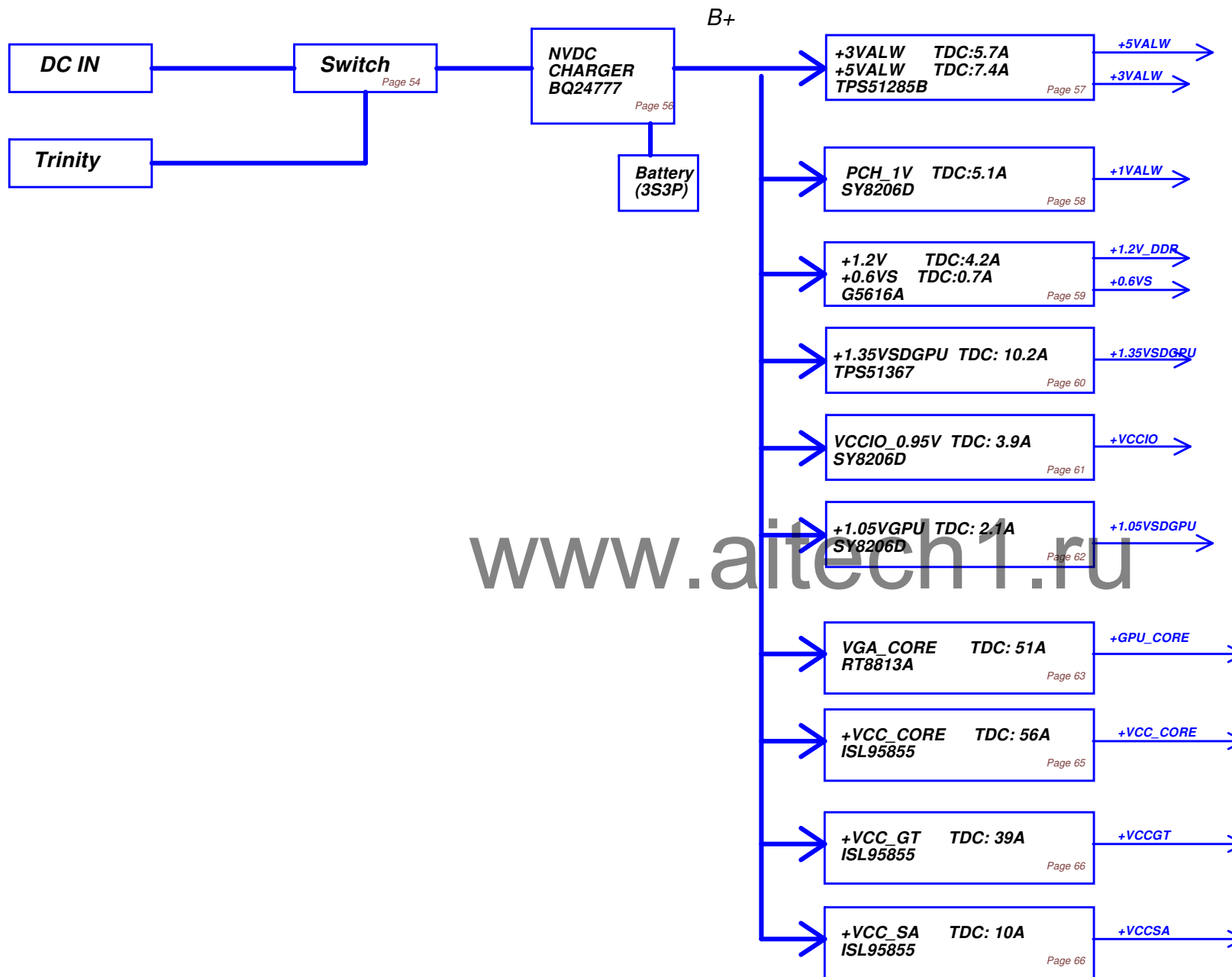
EMI shilding clip x 21

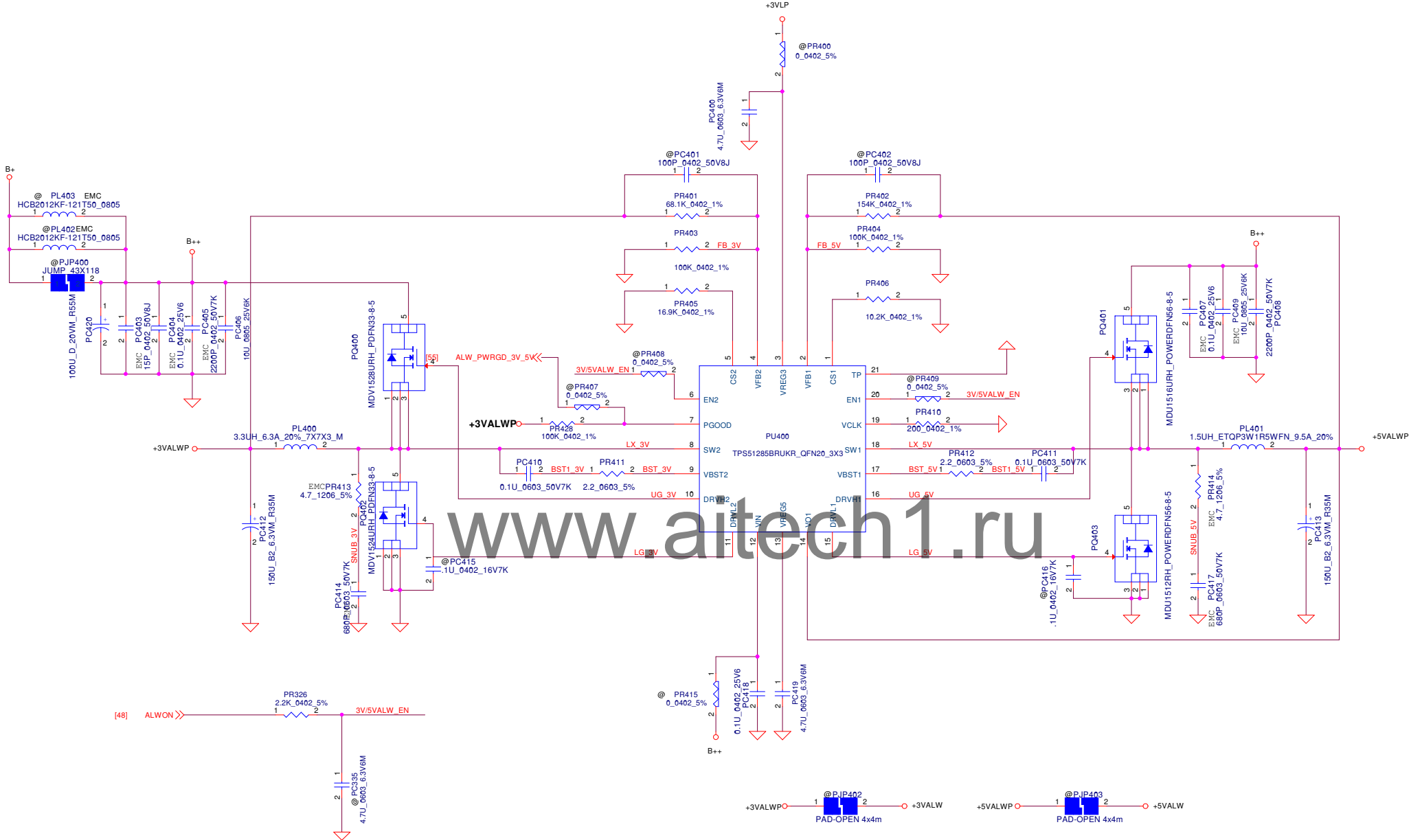


RTC Battery With Charge Function



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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	
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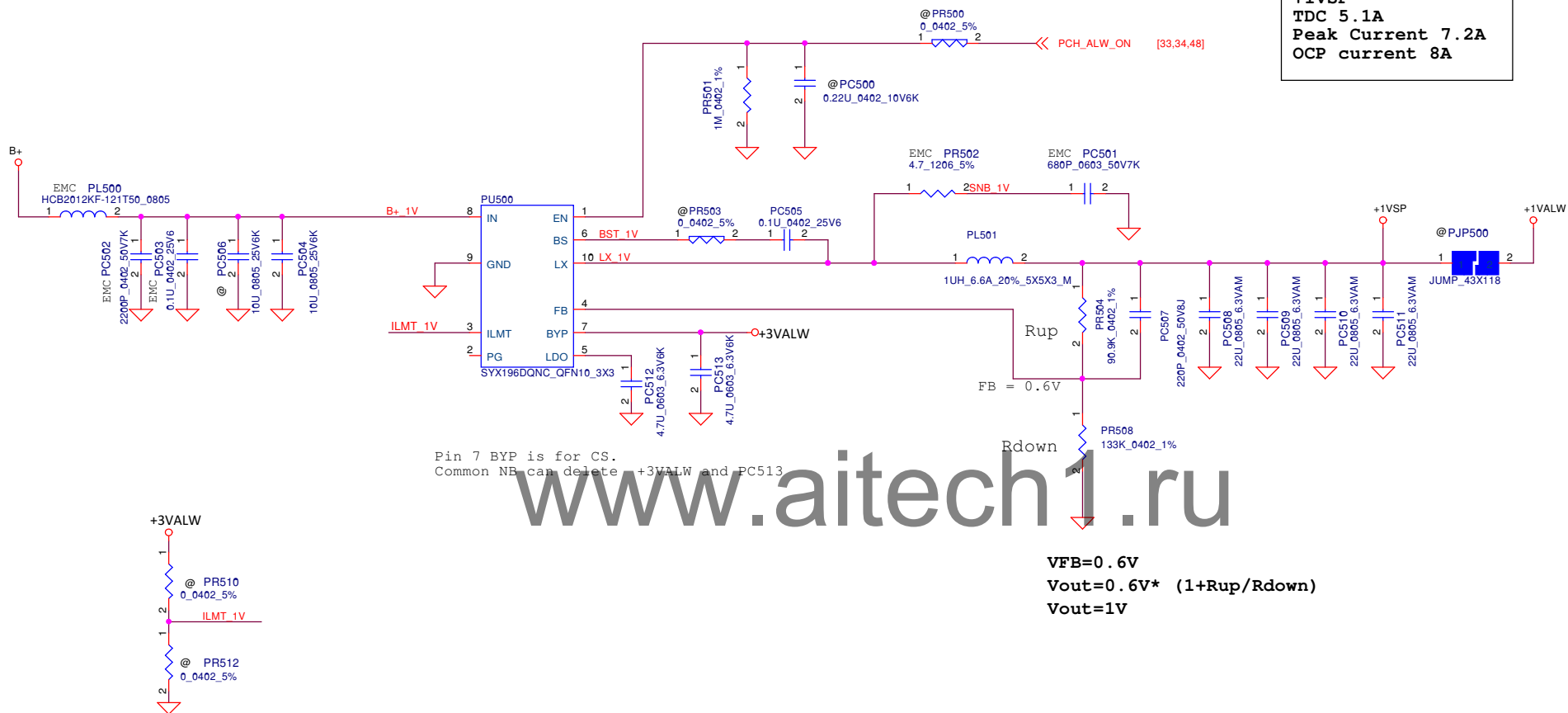


3. 3VALWP
TDC 5.7A
Peak Current 8.1A
OCP current 9.7A

5VALWP
TDC 7.4A
Peak Current 10.5A
OCP current 12.6A

3V/5V controller(35.1), Support component(35.2)

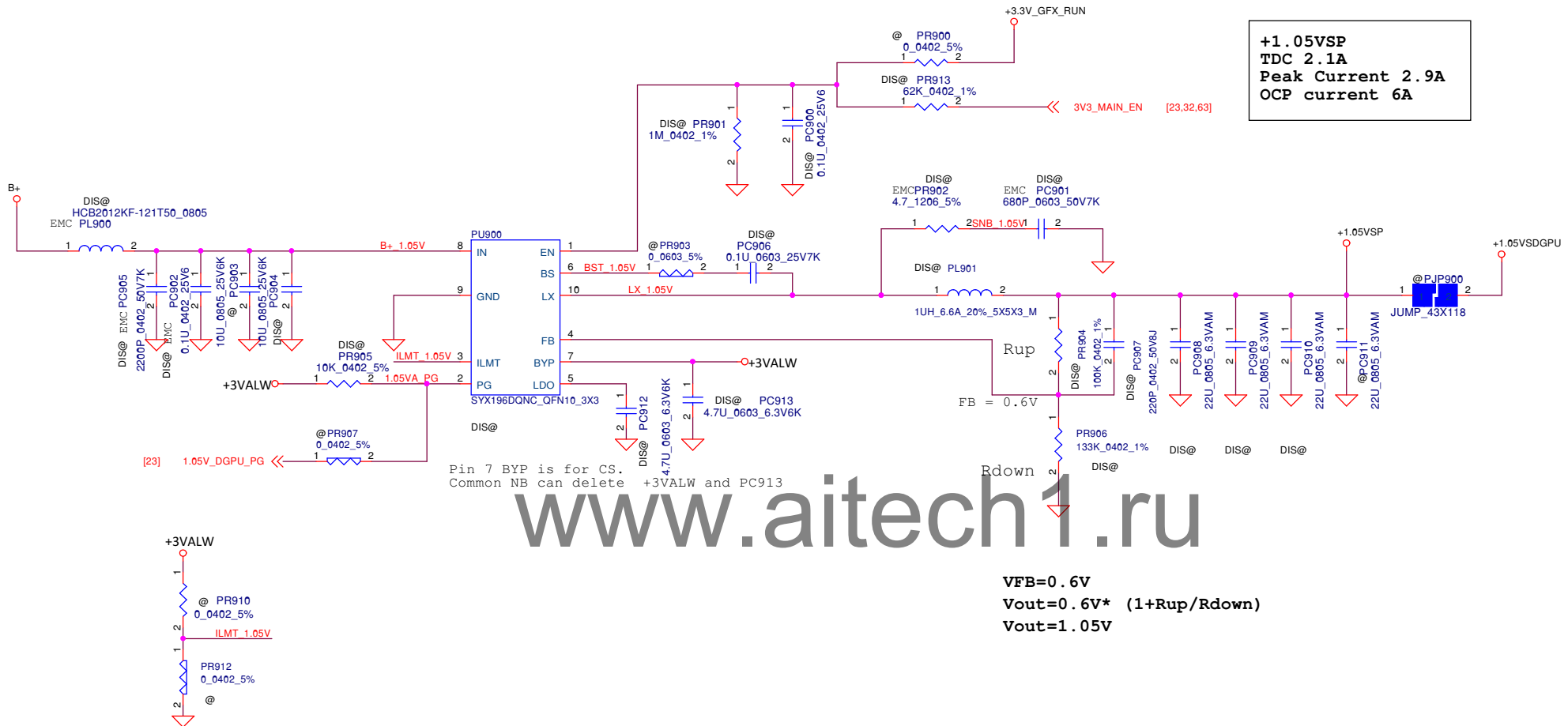
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The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

PWR.Plane.Regulator(35.25), Support component(35.26)

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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P40-PWR +1VA
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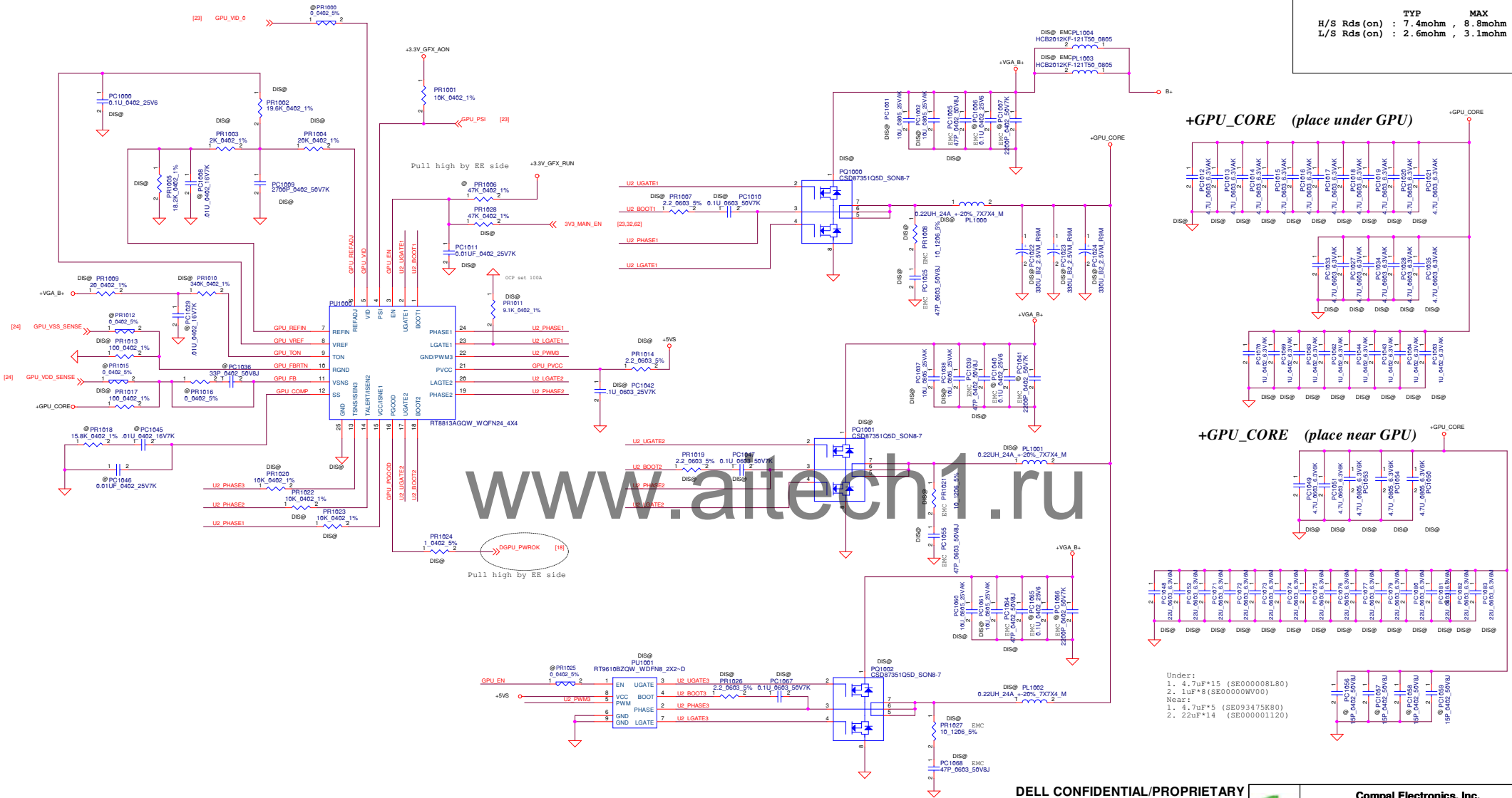


GPU other power_Regulatorr(43.7), Support component(43.8)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P40-PWR +1.05VA
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GPU_CORE (0.95V)
TDC 51A
Peak Current 87A
OCP current 100A
DCR 0.97mohm +/- 5%

TYP MAX
H/S Rds(on) : 7.4mohm , 8.8mohm
L/S Rds(on) : 2.6mohm , 3.1mohm



VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

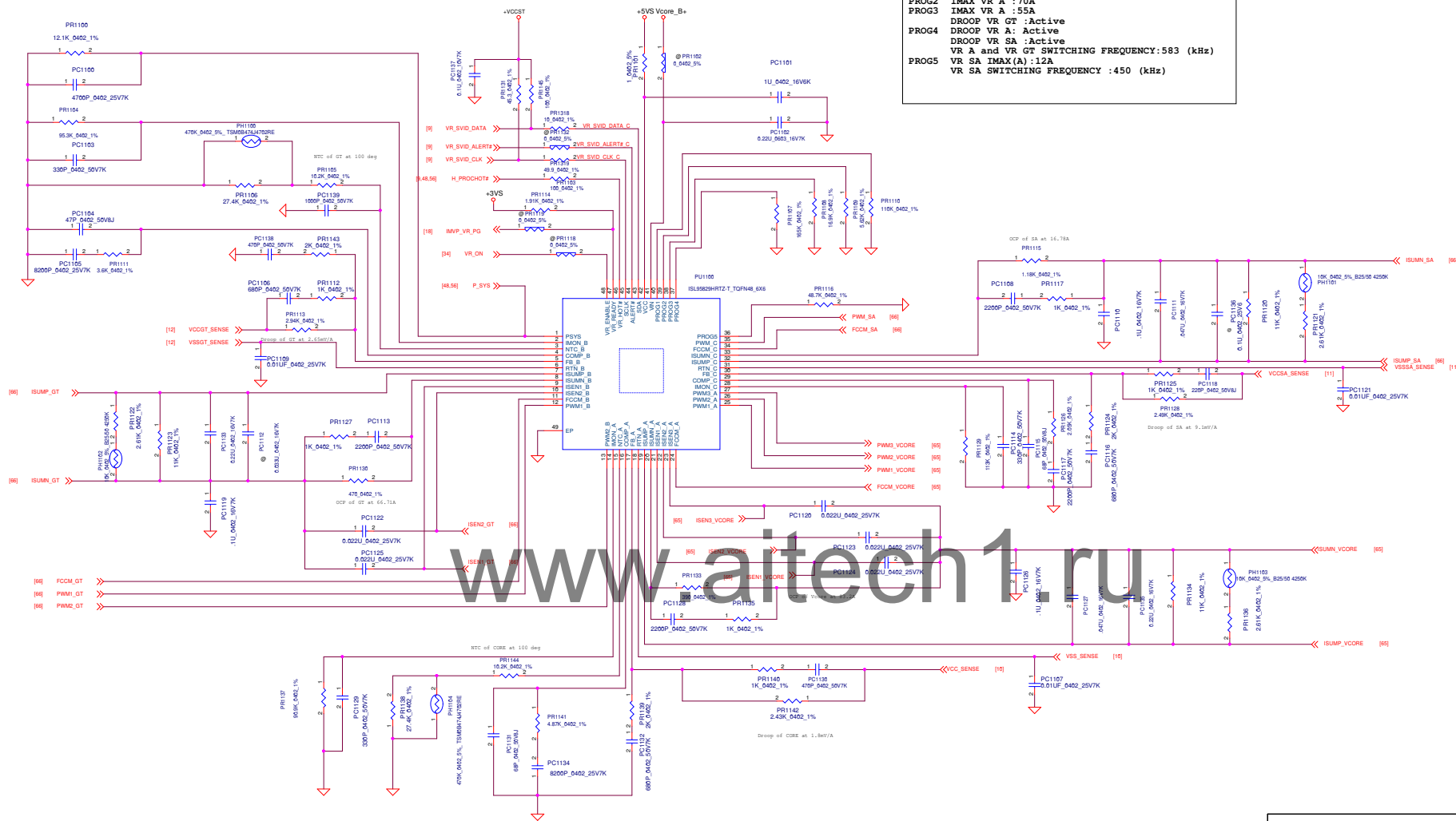
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Compal Electronics, Inc.			
VGA CORE			
LA-C361P			
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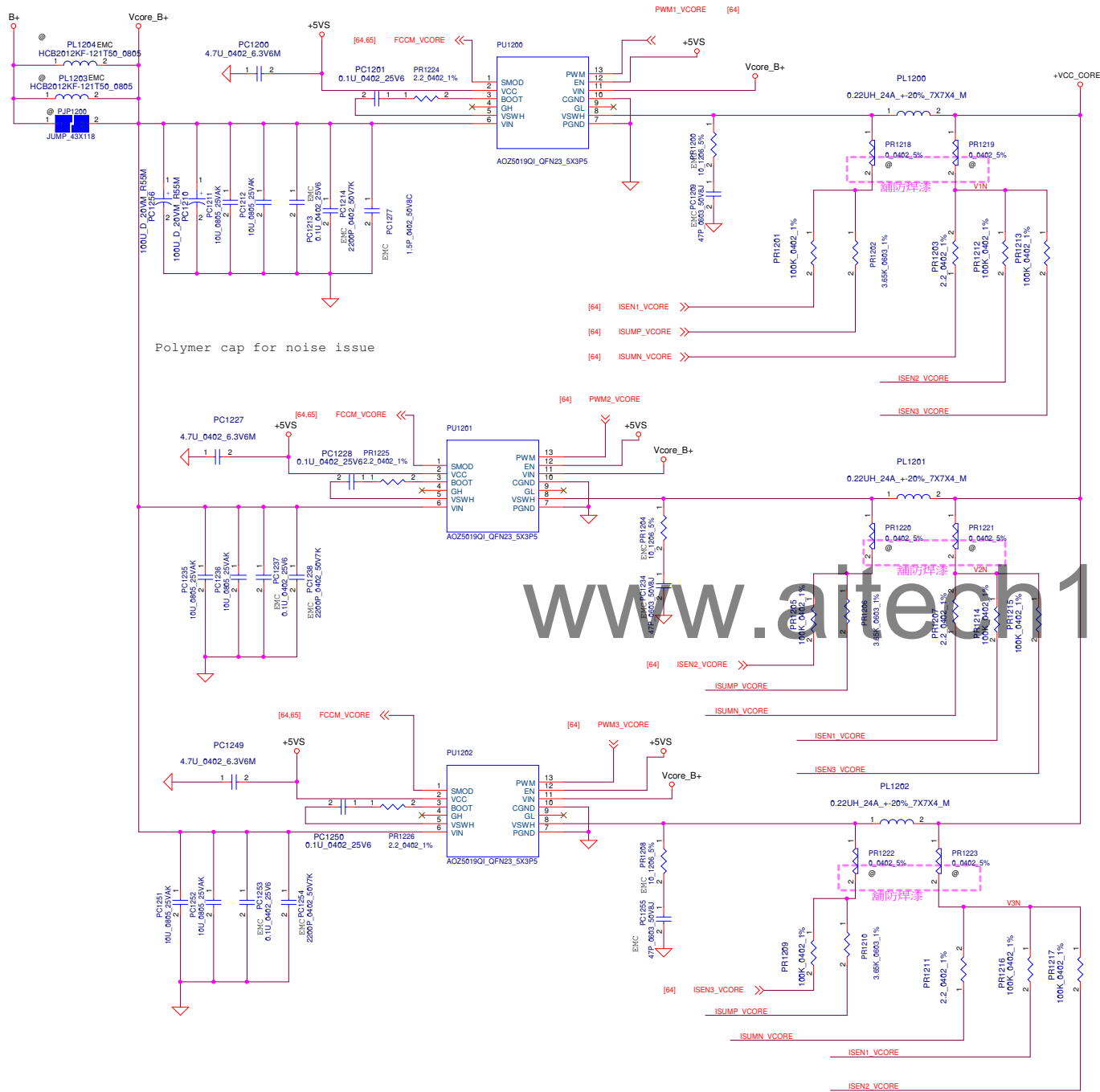
Under:
1. 4.7uF*15 (SE000008L80)
2. 1uF*8 (SE00000WV00)
Near:
1. 4.7uF*5 (SE093475K80)
2. 22uF*14 (SE000001L120)

PROG sets (Base on FNTBD.6 July 25, 2014)
PROG1 Vboot :0V
slew rate :30 mV/uS
PROG2 IMAX VR A :70A
IMAX VR A :55A
PROG3 DROOP VR GT :Active
DROOP VR A :Active
DROOP VR SA :Active
VR A and VR GT SWITCHING FREQUENCY:583 (kHz)
PROG5 VR SA IMAX(A):12A
VR SA SWITCHING FREQUENCY :450 (kHz)



CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3)
Acoustic Noise B+ Bulk CAP(37.2)

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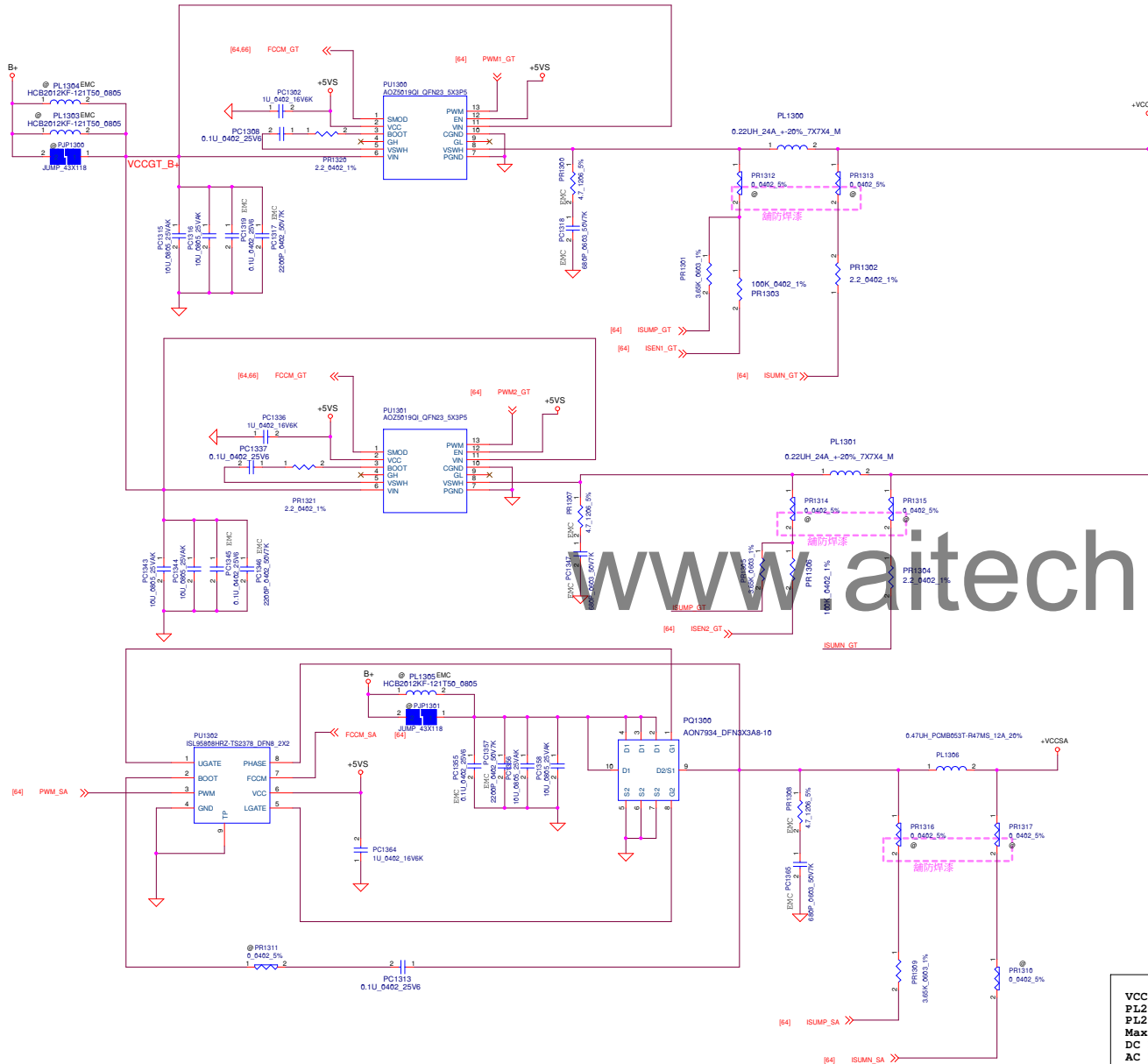
VCC_core (Base on PDDG rev 0.7)
 PL2 TDC_default):TB
 PL2 TDC_max (40Sec):56A
 Peak Current 68A
 DC Load line -1.8mV/A
 AC Load line -1.8mV/A
 OCP Current 83.2A
 DCR 0.97mohm +/-5%

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CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3),
 CPU_Core output CAP(36.4),Acoustic Noise B+ Bulk CAP(37.2)

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VCCGT (Base on PDDG rev 0.7)
 PL2 TDC_default):TB
 PL2 TDC_max (40Sec):39A
 Max Current 55A
 DC Load line -2.65mV/A
 AC Load line -2.65mV/A
 OCP Current 66.7A
 DCR 0.97mohm +/-5%



VCCSA (Base on PDDG rev 0.7)
 PL2 TDC_default):TBD
 PL2 TDC_max (40Sec):10A
 Max Current 11A
 DC Load line -9.1mV/A
 AC Load line -9.1mV/A
 OCP Current 20A
 DCR 7.4mohm/8.5mohm +/-5%

CPU Vcore controller(36.1), Drivers(36.2), Support component(36.3),
 GFX output CAP(36.5)

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Version Change List (P. I. R.

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	XDP	2014/12/12	EE	Change Pull high power for leakage issue	Change RH494,RH495,RH496 from +VCCST to +VCCSTG, dePOP RH97,RH98,RH100, POP RH494,RH495.	X01
2	18	GPIO	2014/12/12	EE	Change Pull high power for double pull high the sam power rail	Change RH571 power rail from +3VS to +V_PCH, de-pop RH571, delete RH532.	X01
3	18	SPI	2014/12/12	EE	Change SPI ROM for ME register setting	Change UH8 from W25Q128FVSIQ_S08 to W25Q128FVSIQ_S0	X01
4	18	S0iX	2014/12/12	EE	Change by pass circuit design for CS mode function	Eange RZ58 connection from UZ11.2 to UZ11.4, ChangeRZ60 connection from UZ12.2 to UZ12.4	X01
5	18	+1V_MPHY	2014/12/12	EE	Delete +1V_MPHY load switch & discharge circuit foruseless.	Delete RH514,RH559,RH144,QH9,UH13,CH193,CH94,CH195. Delete net MPHYP_PWR_EN, move RZ70 to pge 21	X01
6	18	PD	2014/12/22	EE	Update TI PD controller circuit follow Mirama	Update UTS from W25Q80BZPIG_WSON8 to W25Q80DVSSIGS08,Delete RT166,Change net VCC3V3_TBTA_LDO to VCC33_FLASH. Change net VCC3V3_SX_SYS to +3VA_TBTA. Add RT198 to PWR_SRC_TIMUP.Swap UT4_B2/C2 net. Update RT165 from 1206 to 005, RT167,RT168, RT169,RT170,RT171,RT179,RT186,RT187,RT188,RT189,RT32,RT192,RT196,RT197 from 0402 to 0201. Add RT200,RT201 to net UPD_SMBDAT/UPD_SMBCLK"	X01
7	18	EC	2014/12/15	EE	Update Board ID for EC	Update RE67 to 62K	X01
8	18	PM	2014/12/15	EE	modify for support deep sleep function	De-pop RH506	X01
9	18	DDR	2014/12/15	EE	change Power rail for correct design	Change RH525 power rail from +3VALW to +3VS	X01
10	18	SPK	2014/12/15	EE	Add pull high resistor for MB side	Add RH572 to +3VS for SPK_DET#	X01
11	18	GPIO	2014/12/15	EE	Change GPIO for sync common GPIO table	Change net DGPU_PWR_EN from GPP_D13 to GPP_D12	X01
12	18	PD	2014/12/15	EE	Pin swap for DFB review	pin swap DT4,DT9	X01
13	18	PCH	2014/12/15	EE	Add Capacitor for follow Schematic check list	Add CH200 to +3V_PCH (Close to UH2.BA15)	X01
14	18	DIS	2014/12/15	EE	Add pull high resistor by vendor request	Add RPH34 replace to RV520,RV521,RV522 and add netTHERMAL_ALERT#.	X01
15	18	SPI	2014/12/15	EE	Follow CRB XDP design	Add RH574,RH575 for SPI to XDP connector	X01
16	18	VDDQC	2014/12/16	EE	Follow CRB boardfile	POP RH473	X01
17	18	DEBUG	2014/12/16	EE	Add Debug signal by EC request	Change net BID_BC to GPP_C15, Add Net UARTT0_TX fmo GPP_C9 to JDEG1.pin 9	X01
18	18	DEBUG	2014/12/16	EE	Modify Debug UART from closed Chassis toOpen Chassis	Delet UI6,RI29.Add JUART for UART2_TXD/UART2_RXD connect.	X01
19	18	SCI	2014/12/16	EE	Change PU resistor follow Miramar	RH383 change from 100K to 10K	X01
20	18	HOLE	2014/12/16	EE	Add 2 PAD for ME NUT	Add H50, H51	X01
21	18	EC	2014/12/16	EE	Add series resistor follow CRB	Add RE111 43K series S10_SLP_SUS#	X01
22	18	PCH	2014/12/16	EE	Change BOM to follow CRB	Change RH88 from 10K to 47K, De-POP RE33.	X01
23	18	EC	2014/12/17	EE	Modify GPIO for follow GPIO MAP by Dell	Add RE112 and Connect net BID_DIS to UE3.A10, swapNet BAT1_LED#(UE3.B1=>UE3.A40)/BAT2_LED#(UE3.A55=>UE3.B43)/PCH_PCIE_WAKE#(UE3.A40=>UE3.B46)/ME_FWP_EC(UE3.B46=>UE3.B1)/USB_PWR_SHR_LFT_EN#(UE3.B43=>UE3.A55)	X01
24	18	EC	2014/12/17	EE	Update BOM for design change	de-POP RE27, RE63, POP RH453	X01
25	18	NGFF	2014/12/17	EE	Update NGFF from Key E. to Key A.	Change JNGFF1 to CONCR_213AAAA32FA	
26	18	PCH	2014/12/17	EE	Change array resistor to resistor for routing	Change RP21 to RH576,RH577,RH578,RH579. Add RE113,RE114,RE115 for UE1.	
27	18	USB	2014/12/18	EE	Change net name by EC request	USB_PWR_SHR_VBUS_LFT_EN -> USB_PWR_SHR_VBUS_EN_L, SB_PWR_SHR_VBUS_RHT_EN1 -> USB_PWR_SHR_VBUS_EN_R, USB_PWR_SHR_LFT_EN# -> USB_PWR_SHR_EN_L#, USB_PWR_SHR_RHT_EN1# -> USB_PWR_SHR_EN_R#, USB2_DET_EC# -> USB_DET_EC_L#, USB1_DET_EC# -> USBDET_EC_R#	
28	18	TS	2014/12/18	EE	Update Touch Screen Connector by ME request	Update JTS to ACES_50208-00601-P01	
29	18	USB	2014/12/18	EE	Add Pull down resistor for USB2.0	Add RH580,RH581 to UH2.AD10,UH2.AG2 to GND	
30	18	AR	2014/12/19	EE	Reserve test point for Alpine Ridge	Add T199,T200,T201	
31	18	PD	2014/12/22	EE	Delete common mode chok & ESD for vendor feedback	Delete LT10,DT5	
32	18	EC	2014/12/22	EE	Delete I2C signal from EC to Codec.	Delete QE14	
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5				EE			X01
6				EE			X01
7				EE			X01
8				EE			X01
9				EE			X01
10				EE			X01
11				EE			X01
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